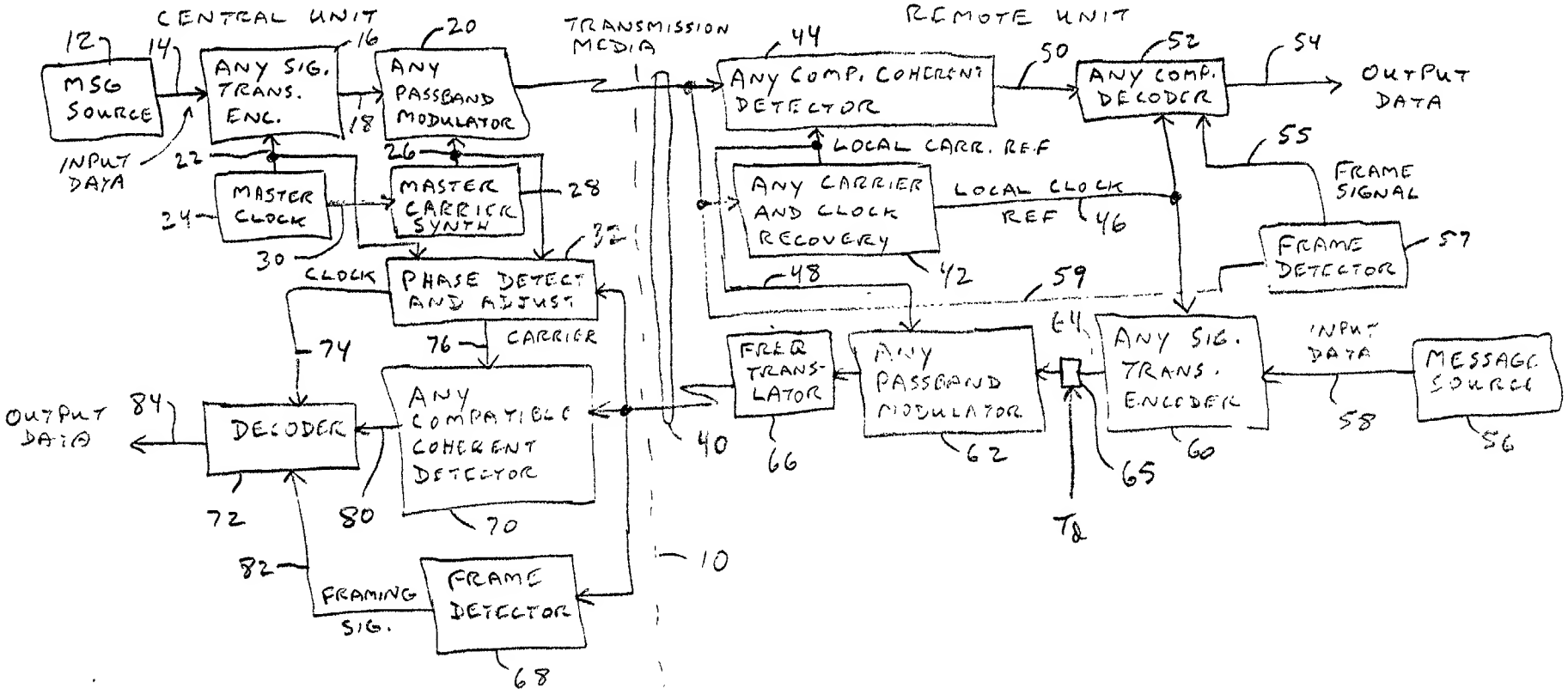
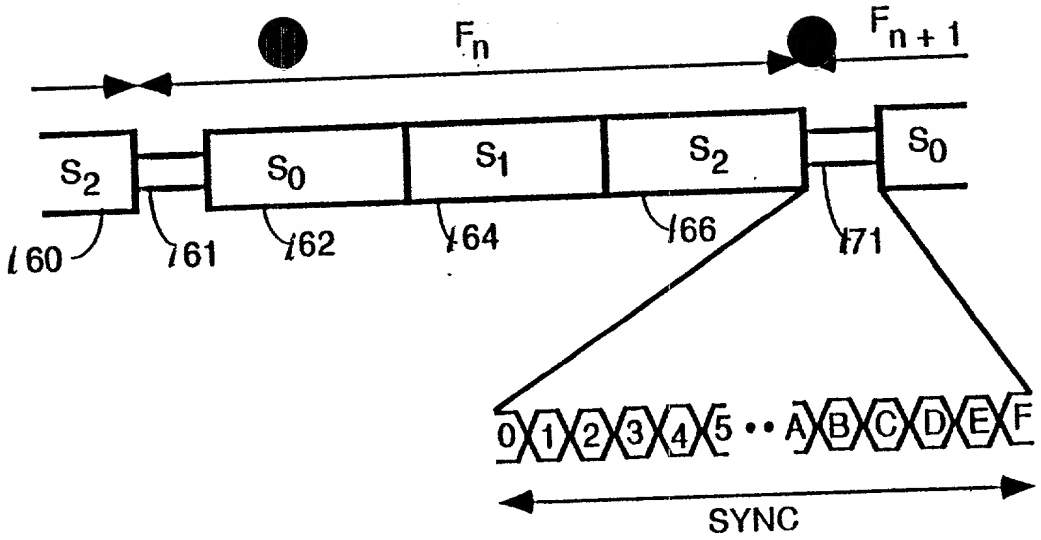
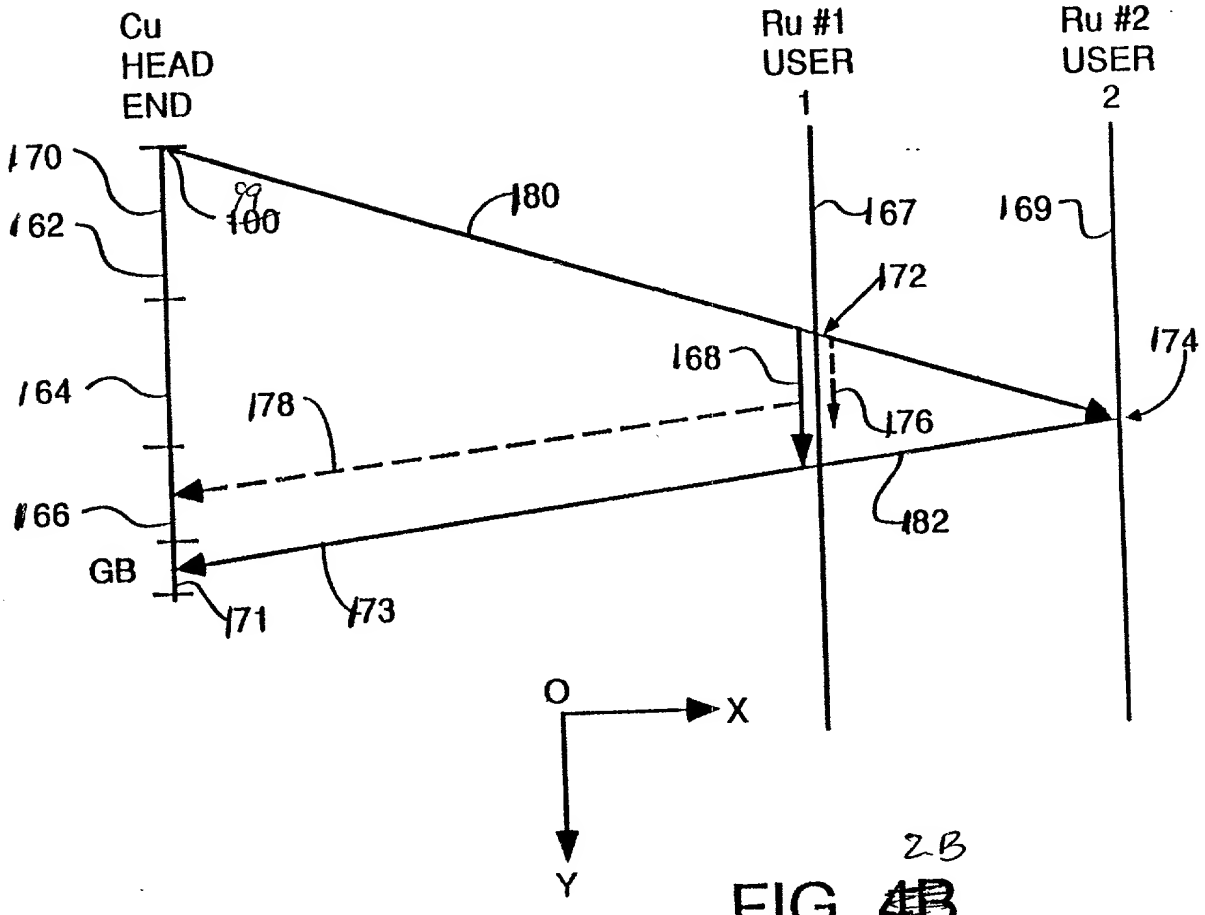

CENTRAL UNIT
REMOTE UNIT
TRANSMISSION MEDIA
MSG SOURCE
ANY SIG. TRANS. ENC.
ANY PASSBAND MODULATOR
INPUT DATA
MASTER CLOCK
MASTER CARRIER SYNTH
PHASE DETECT AND ADJUST
CLOCK
CARRIER
DECODER
OUTPUT DATA
ANY COMPATIBLE COHERENT DETECTOR
FRAME DETECTOR
FRAMING SIG.
ANY COMP. COHERENT DETECTOR
LOCAL CARR. REF
ANY CARRIER AND CLOCK RECOVERY
LOCAL CLOCK REF
ANY COMP. DECODER
OUTPUT DATA
FRAME SIGNAL
FRAME DETECTOR
FREQ TRANS-LATOR
ANY PASSBAND MODULATOR
ANY SIG. TRANS. ENCODER
INPUT DATA
MESSAGE SOURCE
12
14
16
18
20
22
24
26
28
30
32
40
42
44
46
48
50
52
54
55
57
59
60
62
64
65
66
70
72
74
76
80
82
84
56
58
10
T&

FIG. 1



2A

FIG. 4A



2B

FIG. 4B

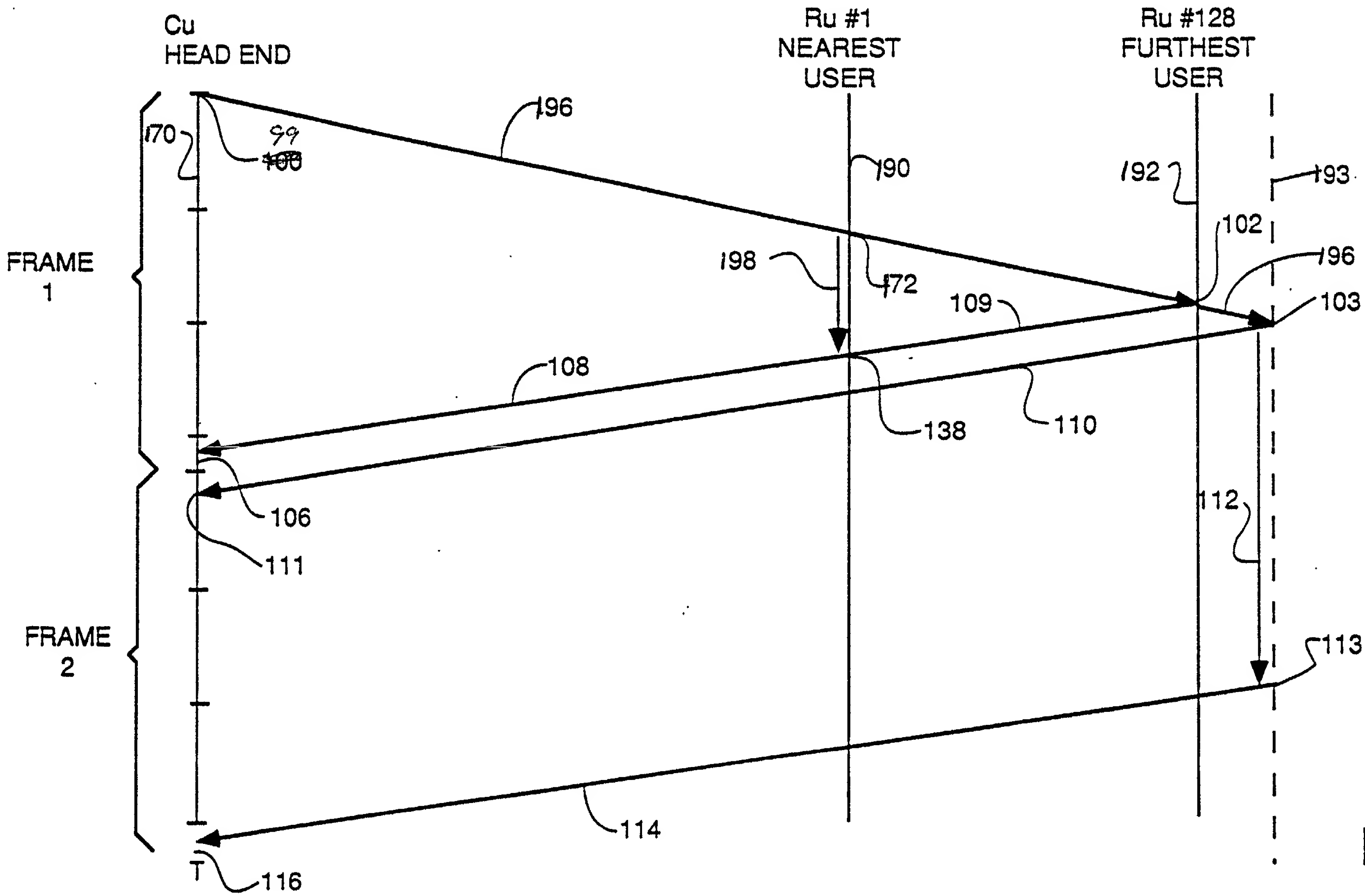

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
1
FRAME
2
196
99
170
190
192
193
102
196
198
172
109
103
108
138
110
106
111
112
113
114
T
116

FIG. 3

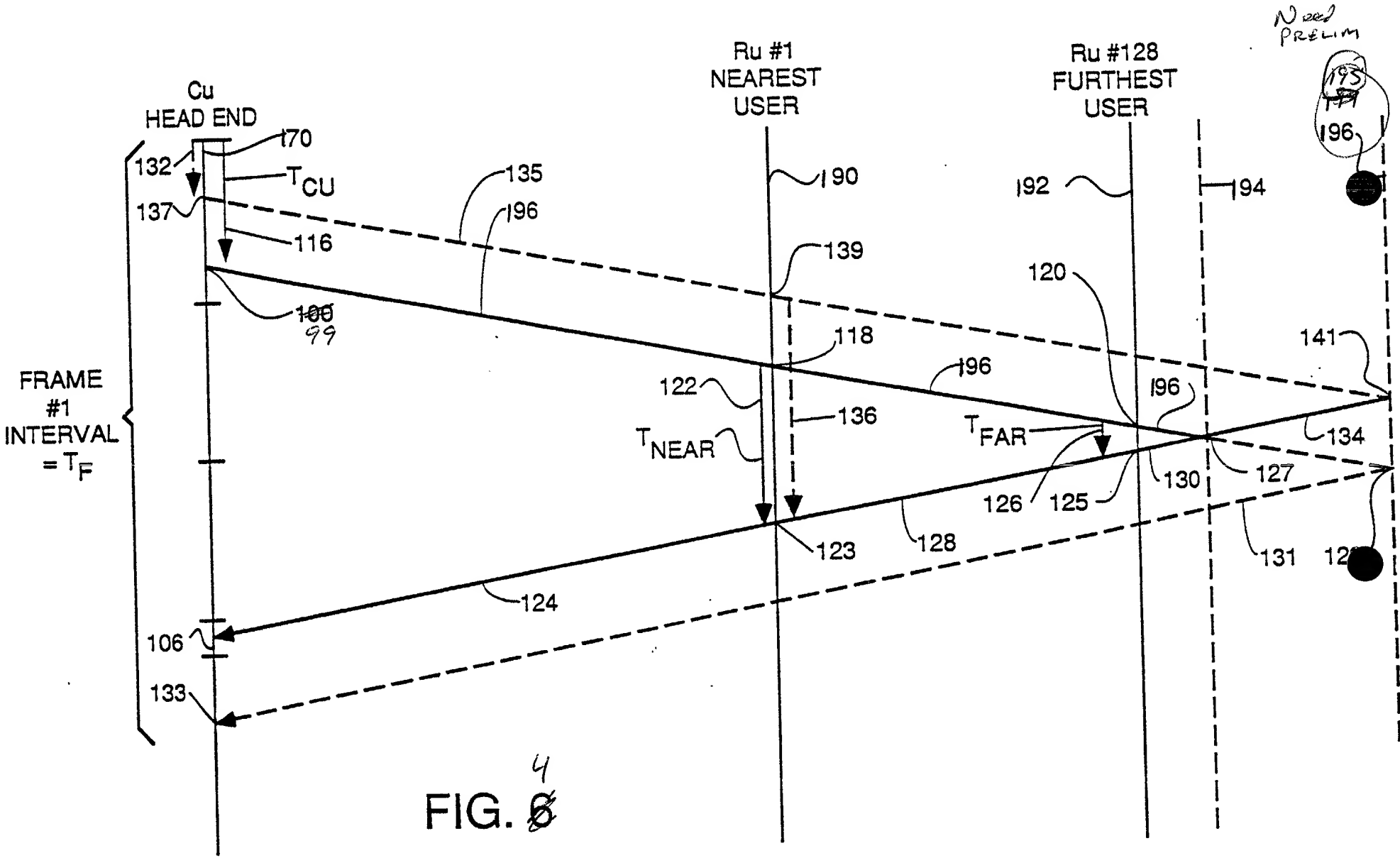
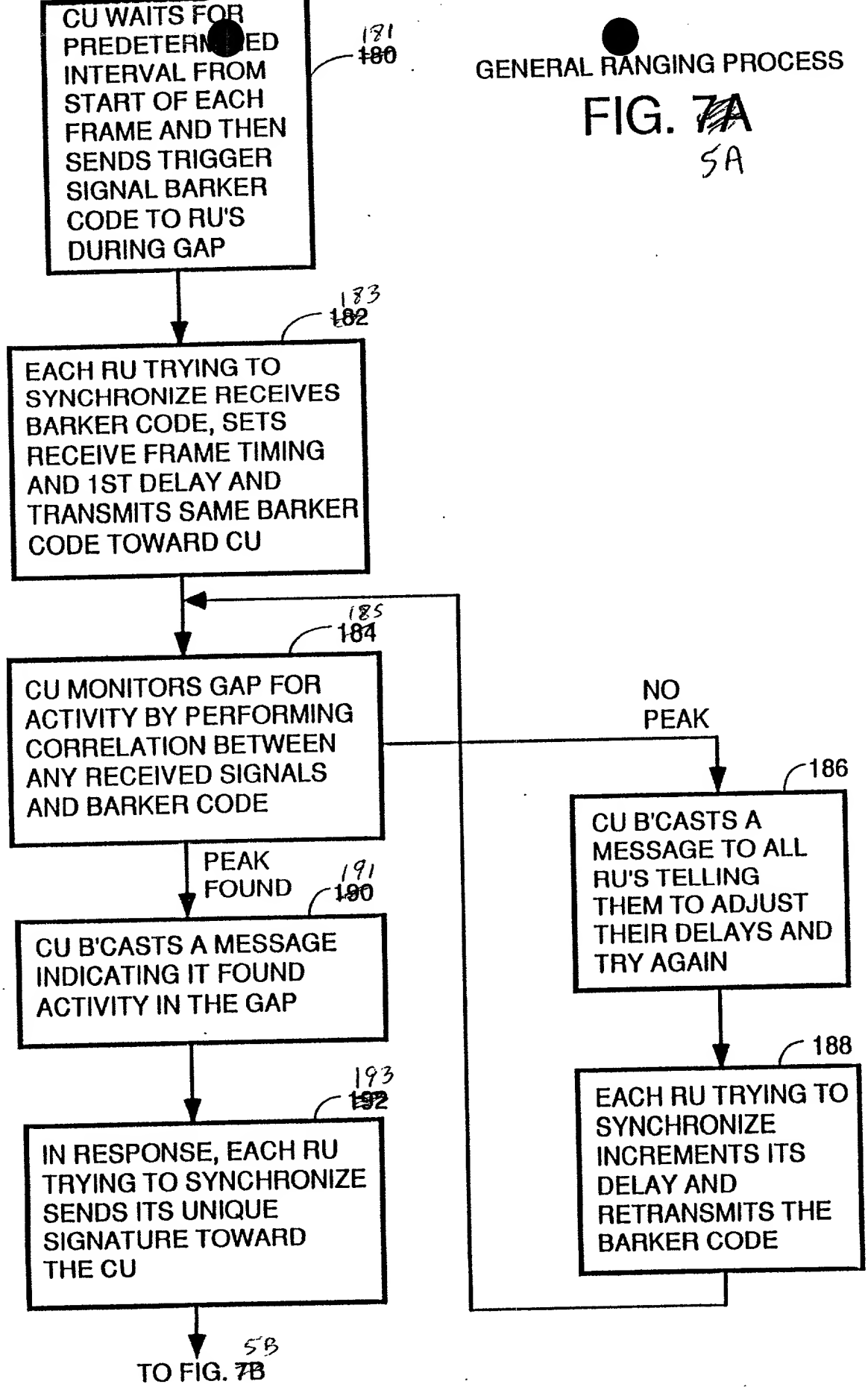
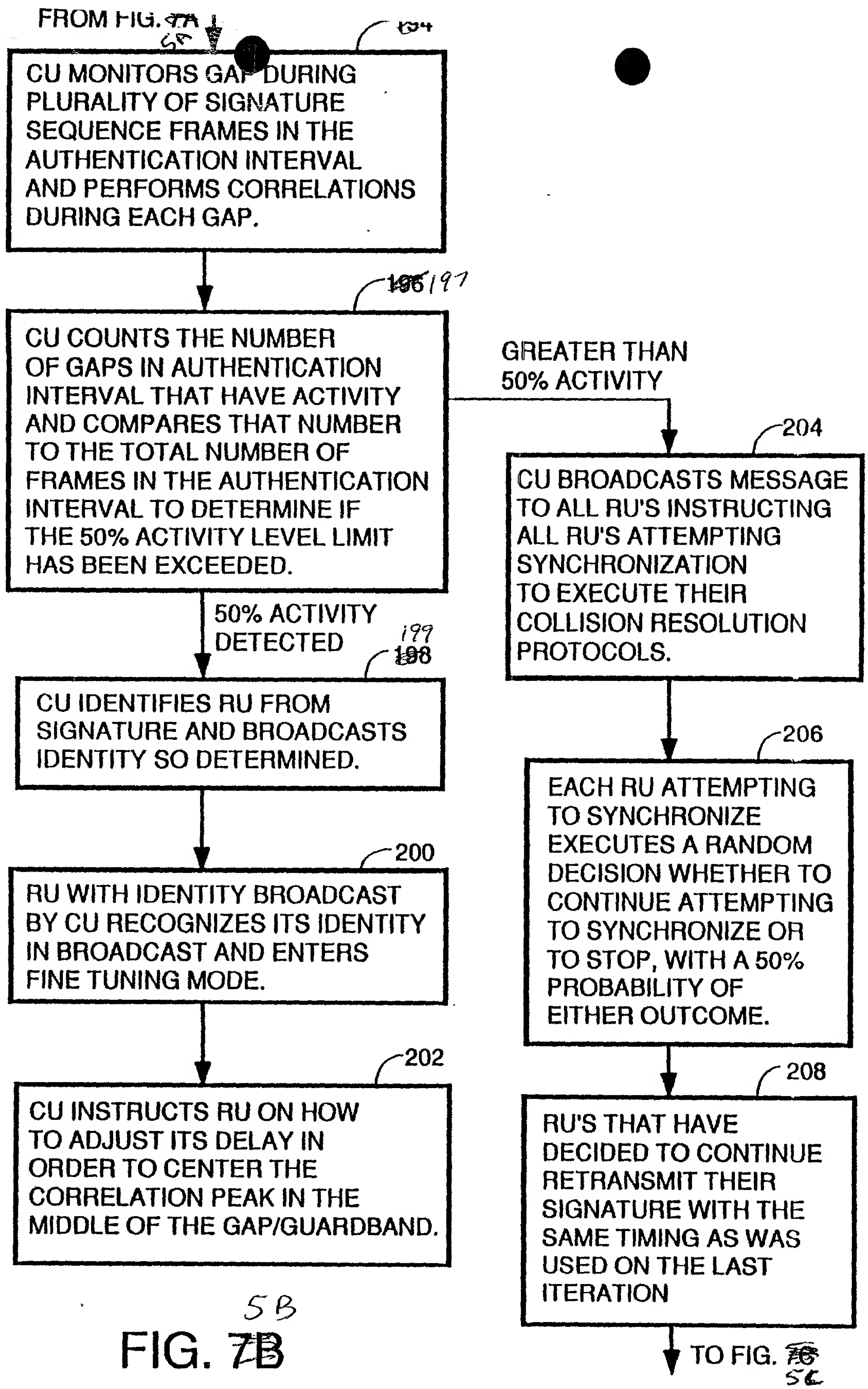

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
#1
INTERVAL
= T_F
T_{CU}
T_{NEAR}
T_{FAR}
170
132
137
116
135
196
190
139
118
122
136
192
194
120
141
134
127
130
126
125
123
128
131
124
106
133

FIG. 4

GENERAL RANGING PROCESS

FIG. ~~7A~~ 5A




FROM FIG. 7A 5A
194
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
196 197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
50% ACTIVITY DETECTED
198 199
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 7C 5C

5B

FIG. 7B

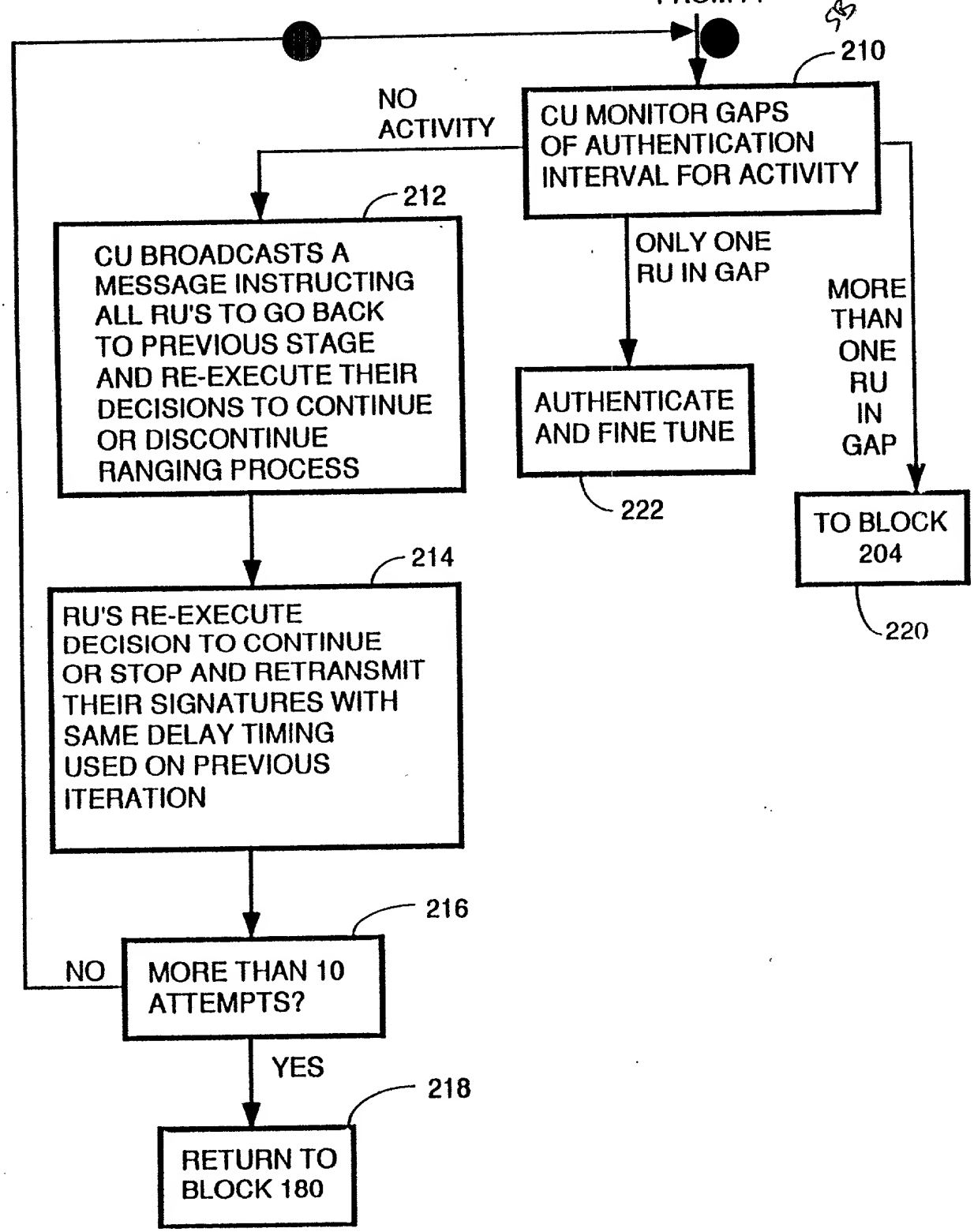
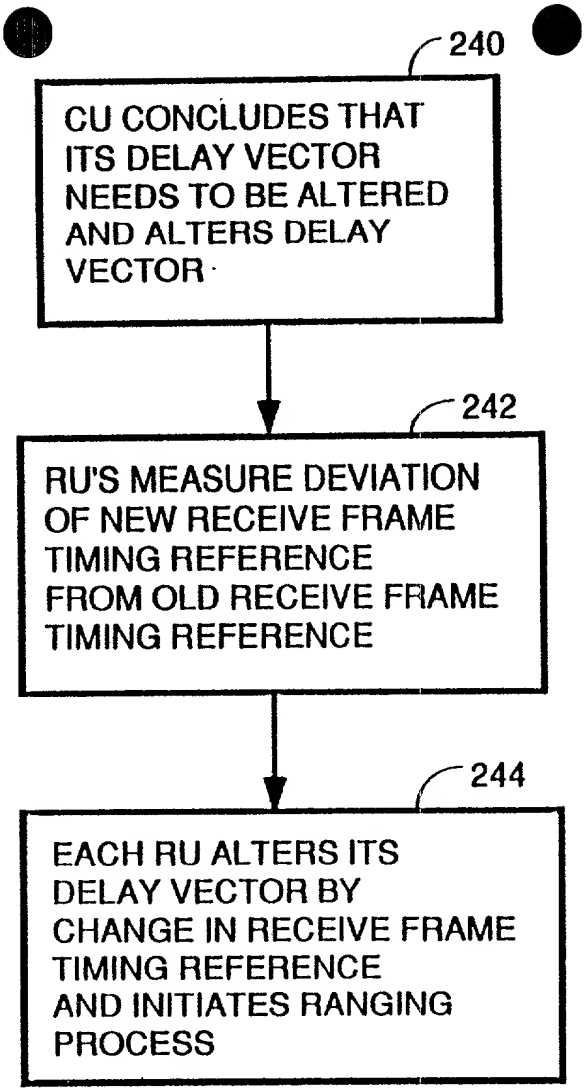

210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
ONLY ONE RU IN GAP
MORE THAN ONE RU IN GAP
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
AUTHENTICATE AND FINE TUNE
222
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C ~~7C~~



6

FIG. 8

DEAD RECKONING RE-SYNC

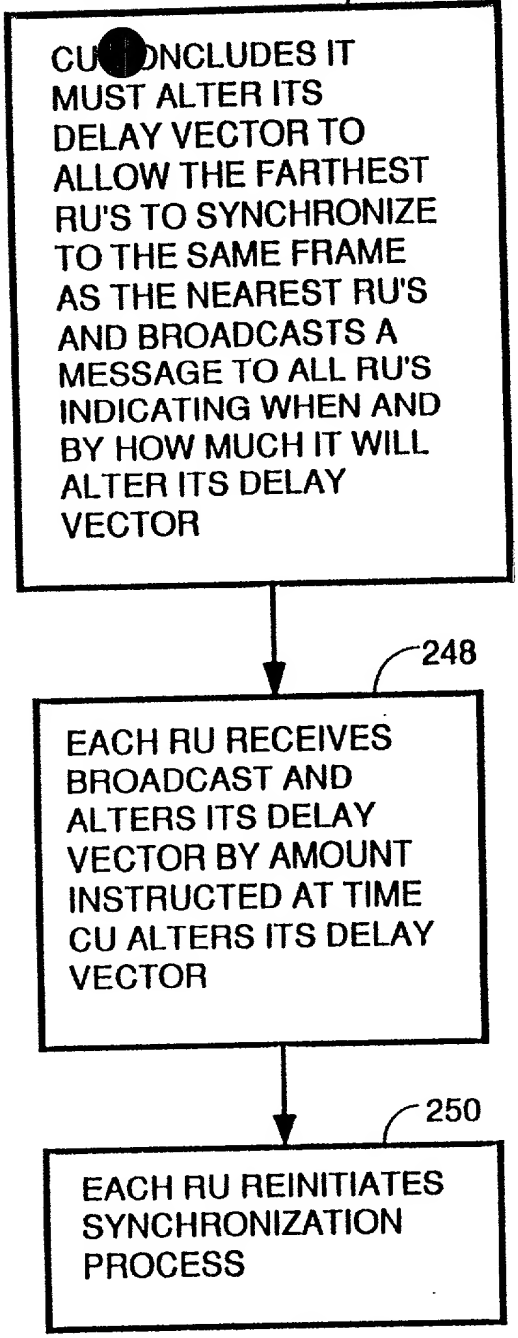
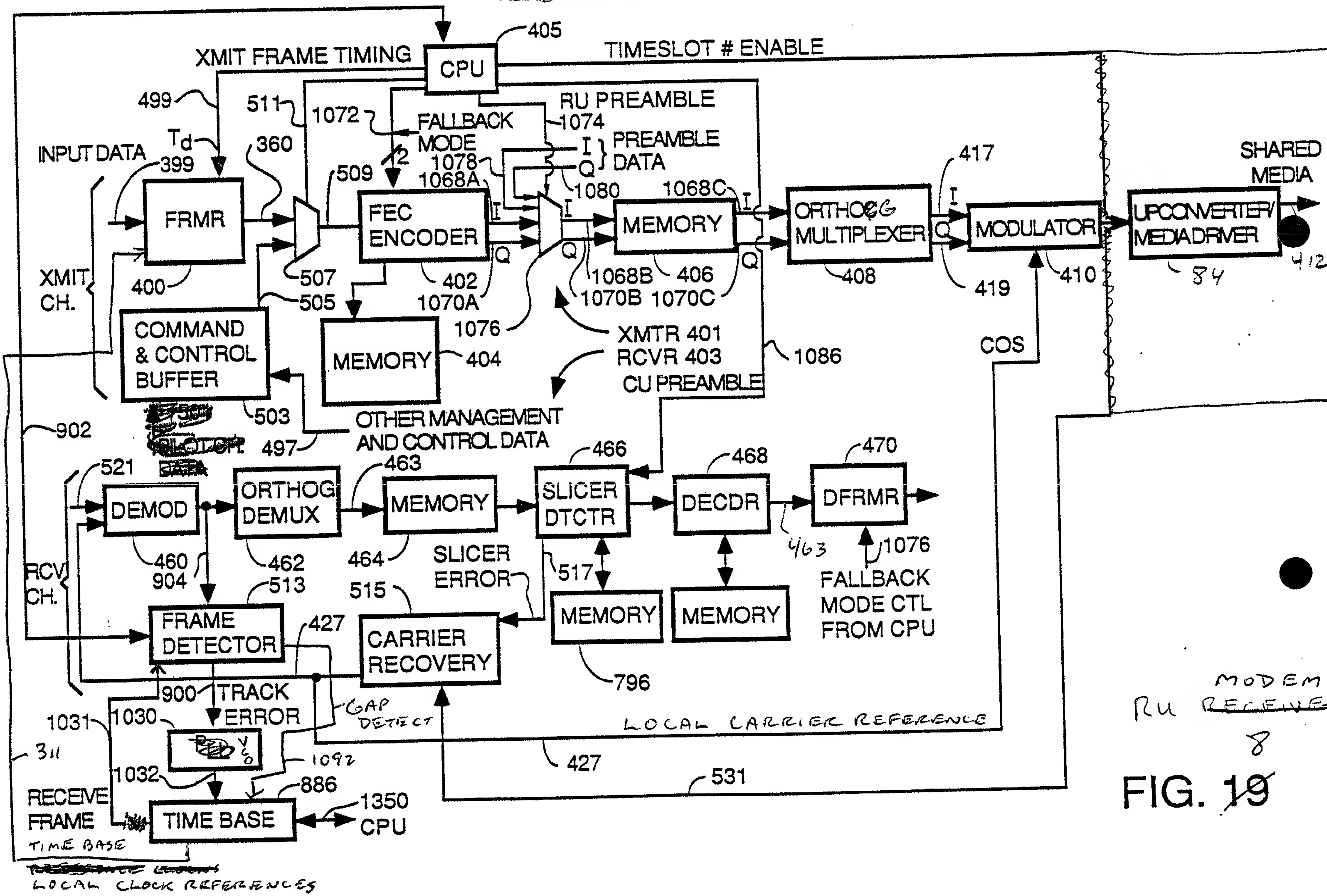


FIG. 9

PRECURSOR EMBODIMENT

RU DIGITAL MODEM BLOCK DIAGRAM



MODEM RU RECEIVE

FIG. 8

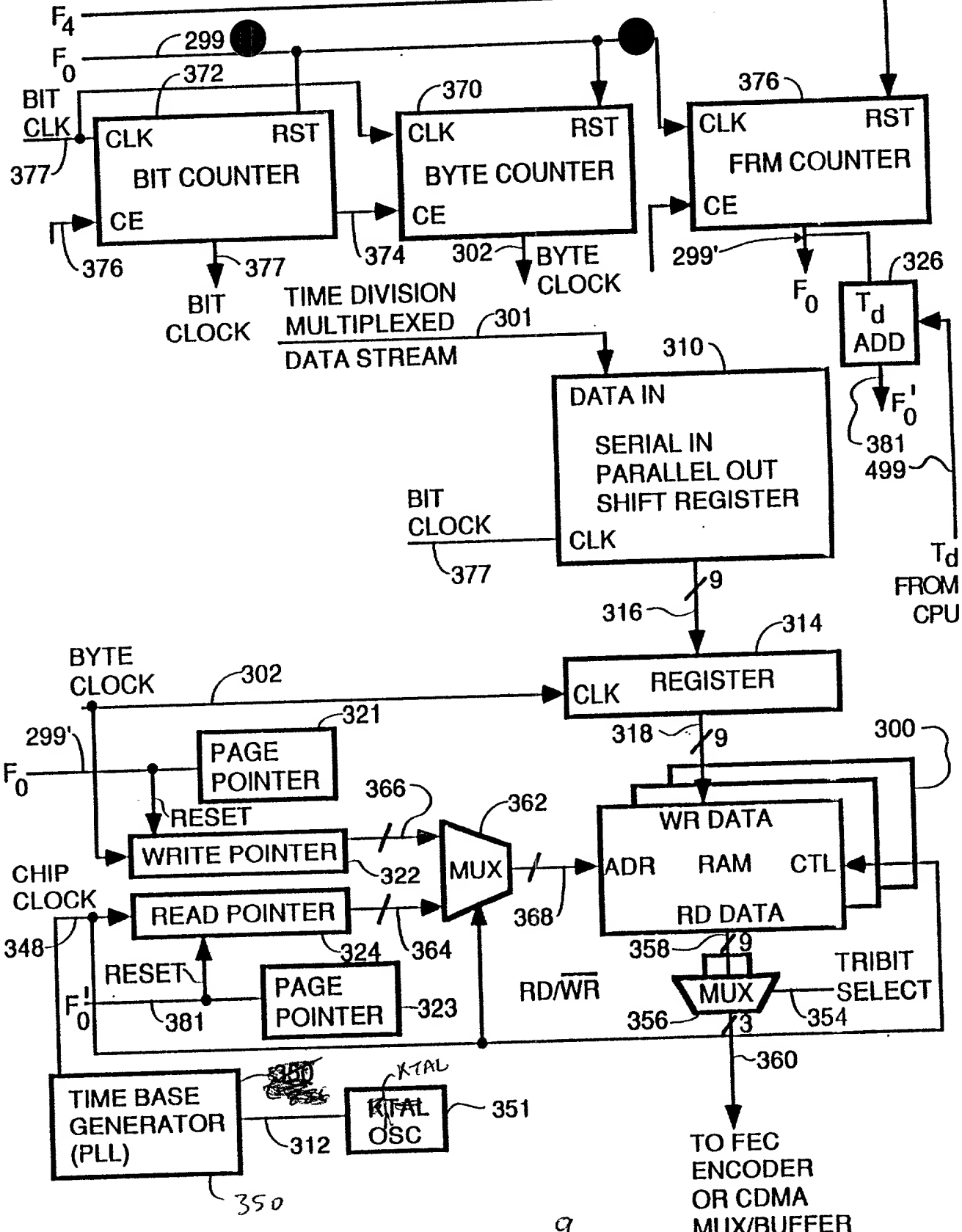

F4
F0
299
372
370
376
BIT CLK
377
CLK RST
BIT COUNTER
CE
376
377
374
CLK RST
BYTE COUNTER
CE
302
BYTE CLOCK
CLK RST
FRM COUNTER
CE
299'
F0
326
Td ADD
F'0
381
499
BIT CLOCK
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
CLK
BIT CLOCK
377
9
316
314
Td FROM CPU
BYTE CLOCK
302
CLK REGISTER
321
299'
F0
PAGE POINTER
RESET
318
9
300
366
362
WRITE POINTER
322
MUX
WR DATA
ADR RAM CTL
RD DATA
CHIP CLOCK
348
READ POINTER
324
364
368
358
9
TRIBIT SELECT
RESET
F'0
381
PAGE POINTER
323
RD/WR
MUX
356
3
354
360
TIME BASE GENERATOR (PLL)
312
XTAL OSC
351
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 12

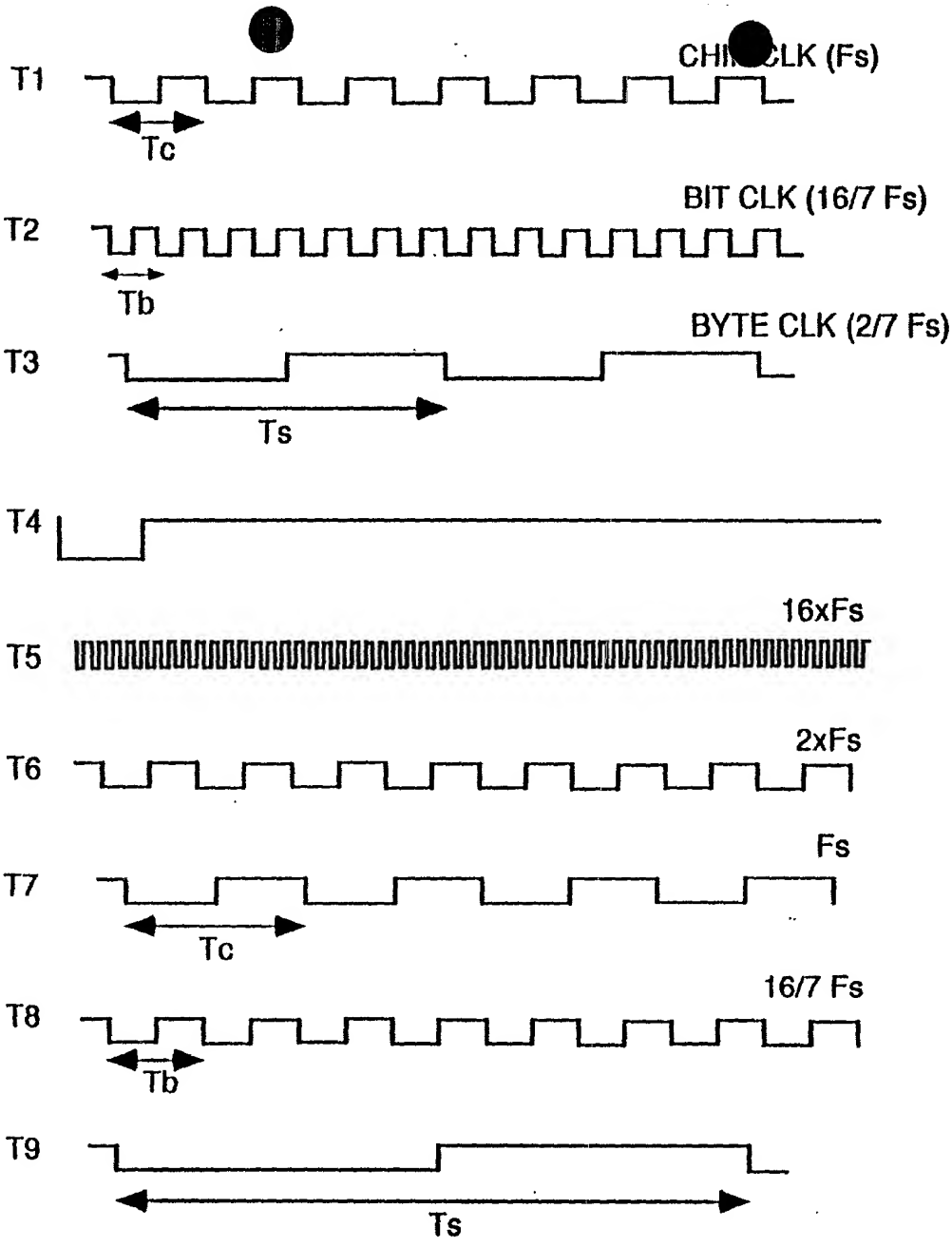
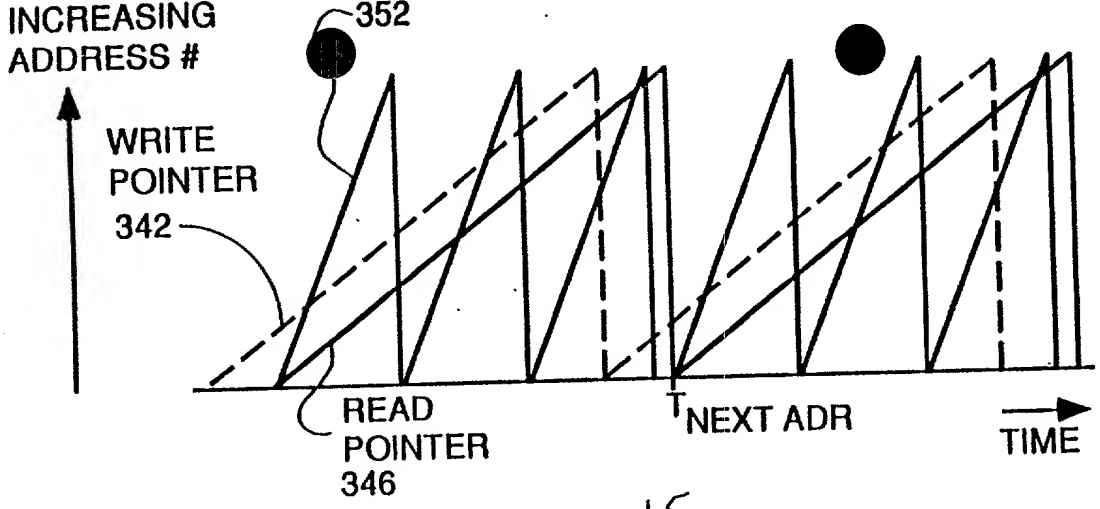
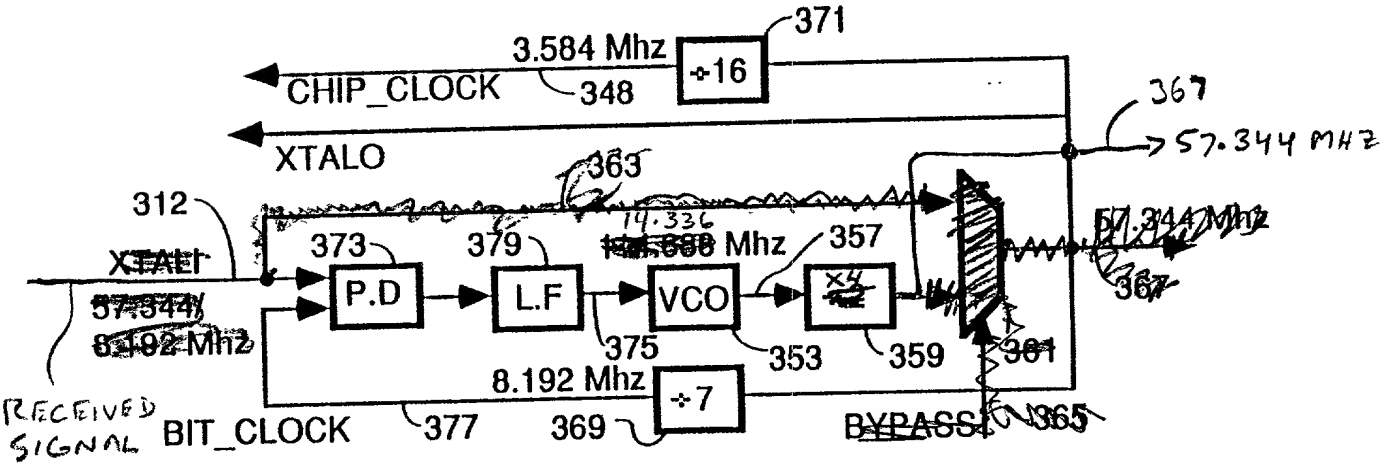

T1
CHI CLK (Fs)
Tc
T2
BIT CLK (16/7 Fs)
Tb
T3
BYTE CLK (2/7 Fs)
Ts
T4
T5
16xFs
T6
2xFs
T7
Fs
Tc
T8
16/7 Fs
Tb
T9
Ts

FIG. 10/13



15

FIG. 17



11

FIG. 18

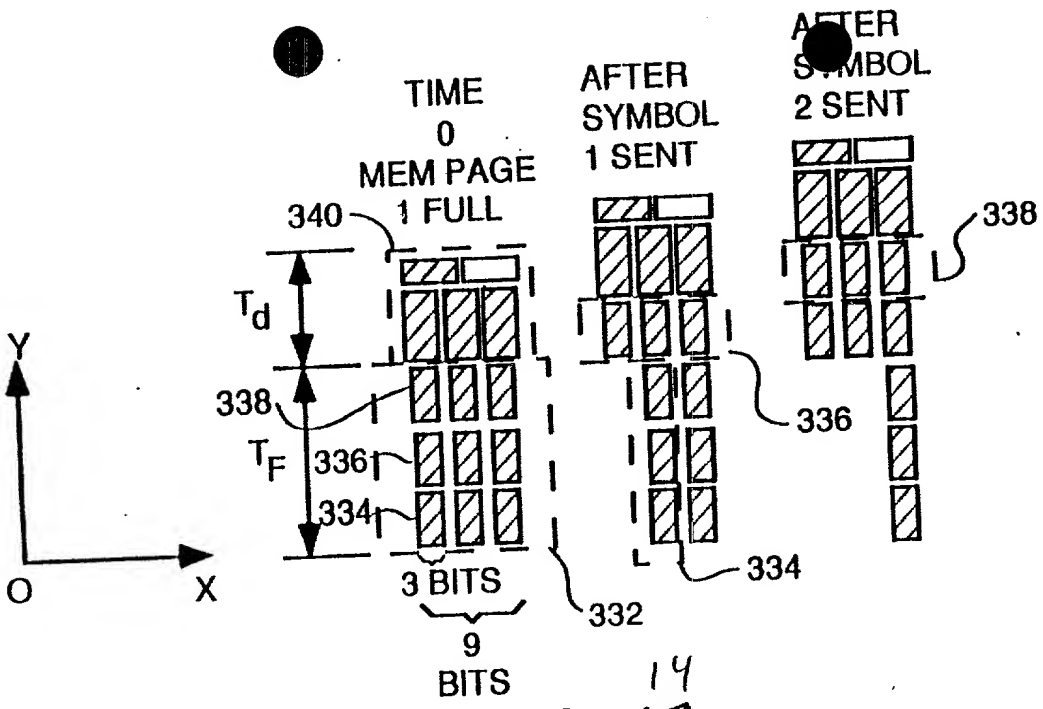


FIG. 14

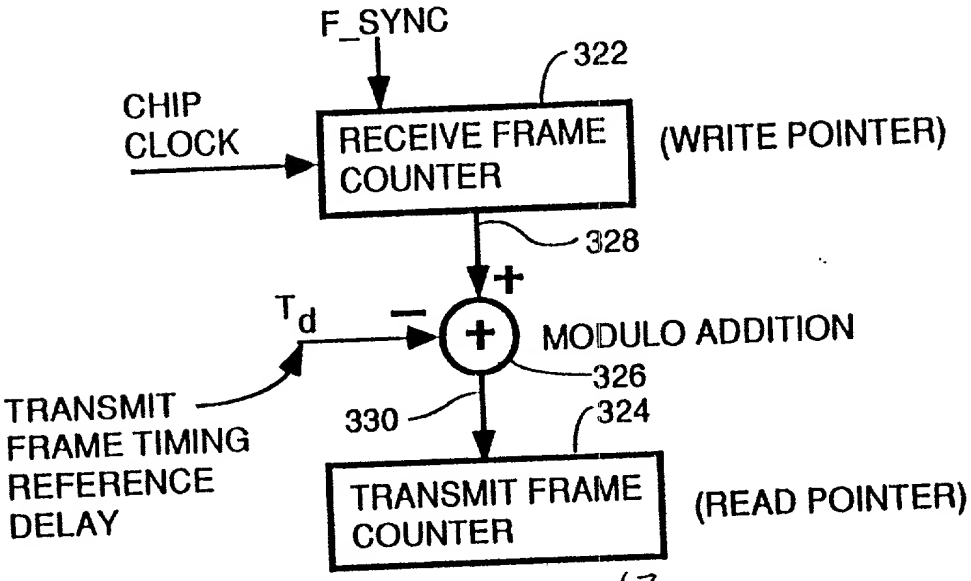


FIG. 15

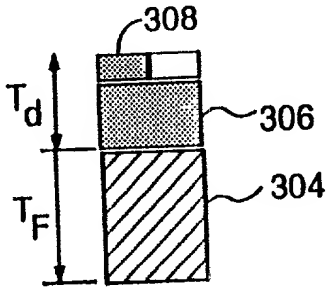
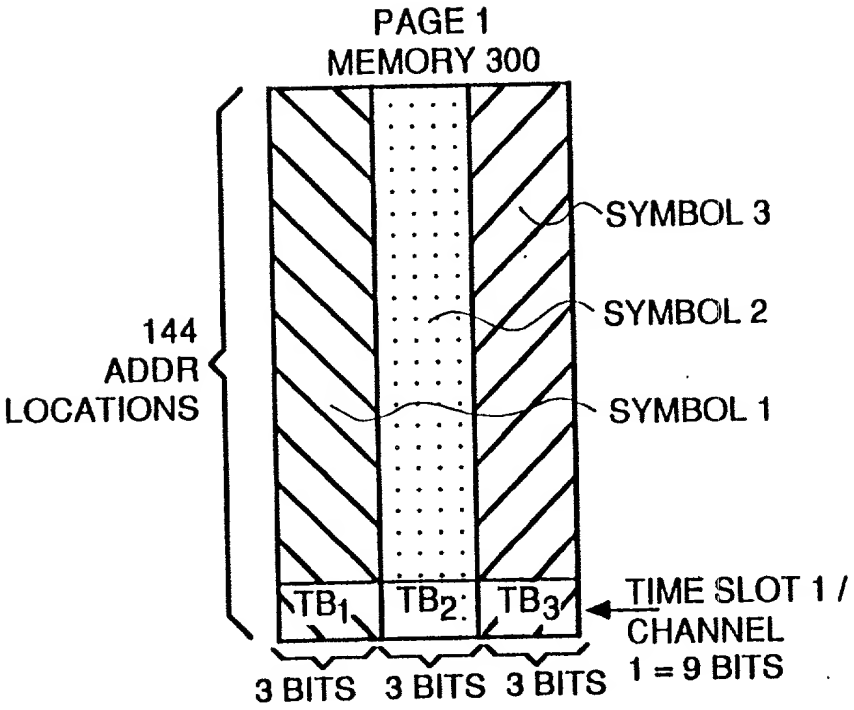
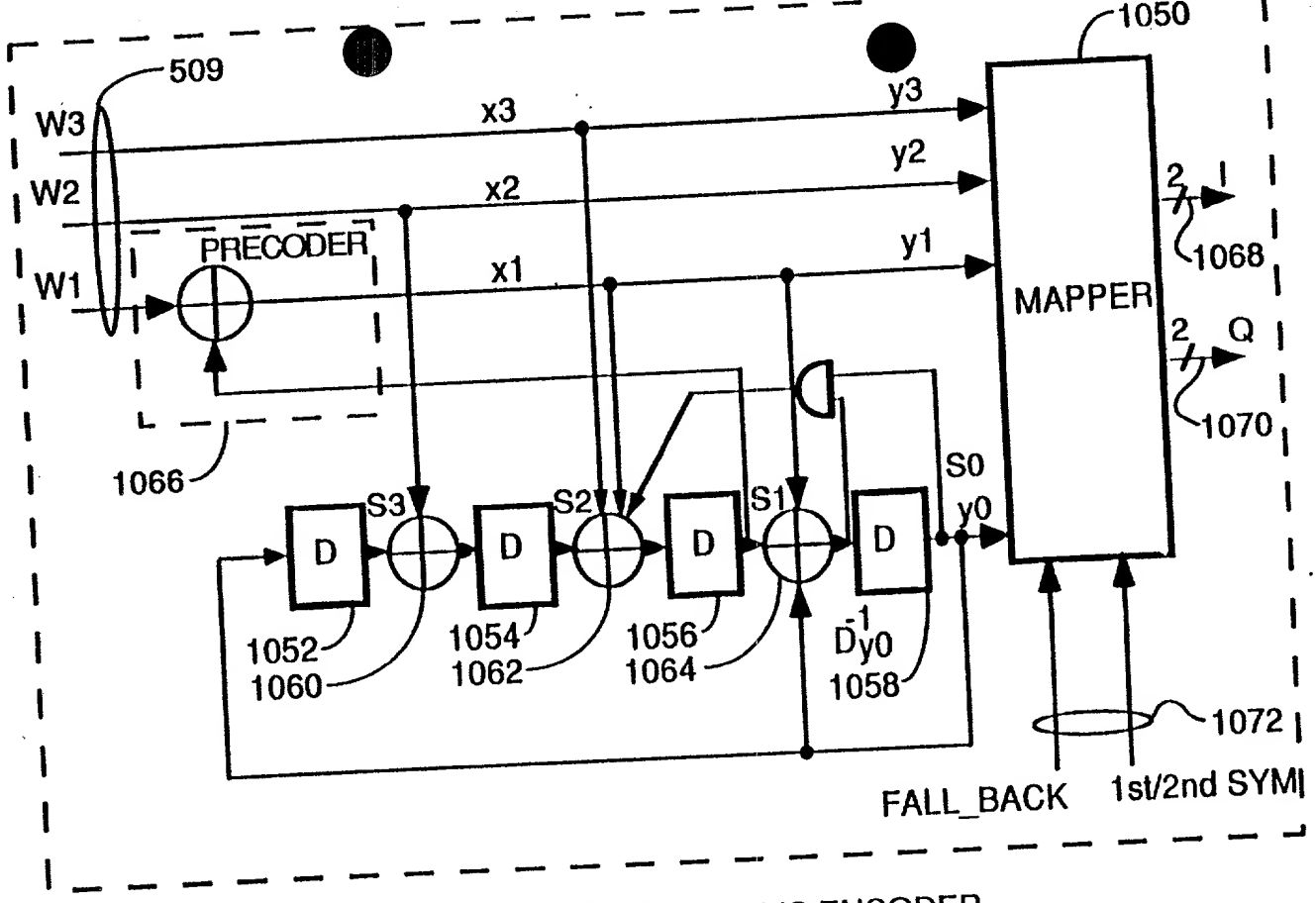


FIG. 16


PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

16

FIG. 20

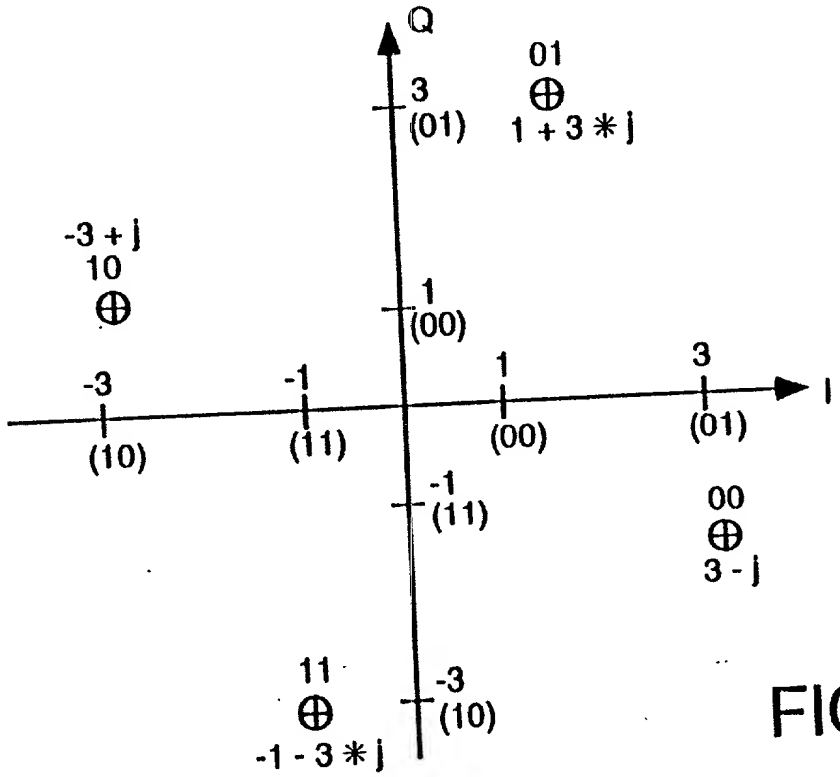


PREFERRED TRELLIS ENCODER

FIG. 42

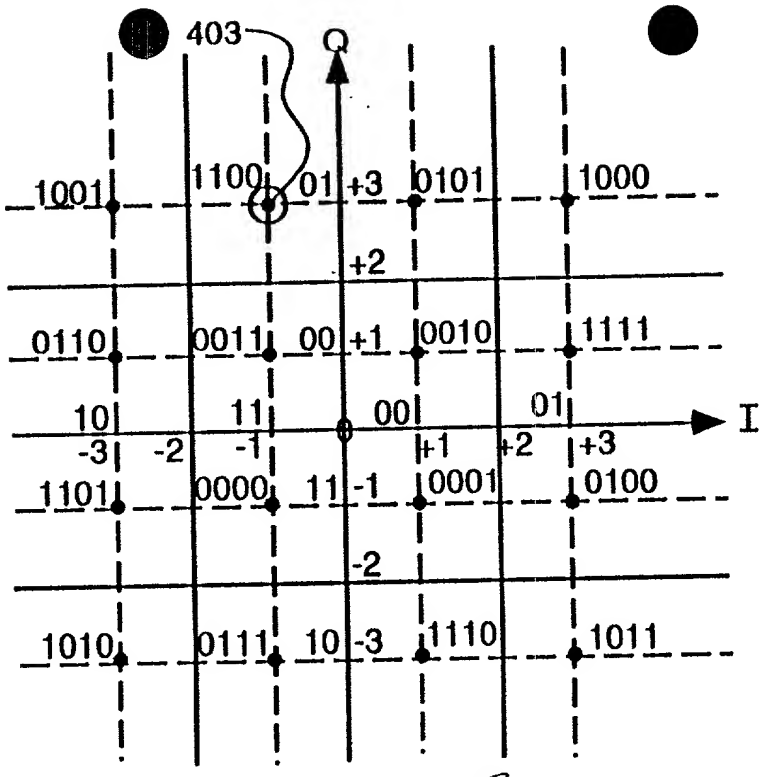
17

MAPPING FOR FALL-BACK MODE - LSB'S



21

FIG. 43



18

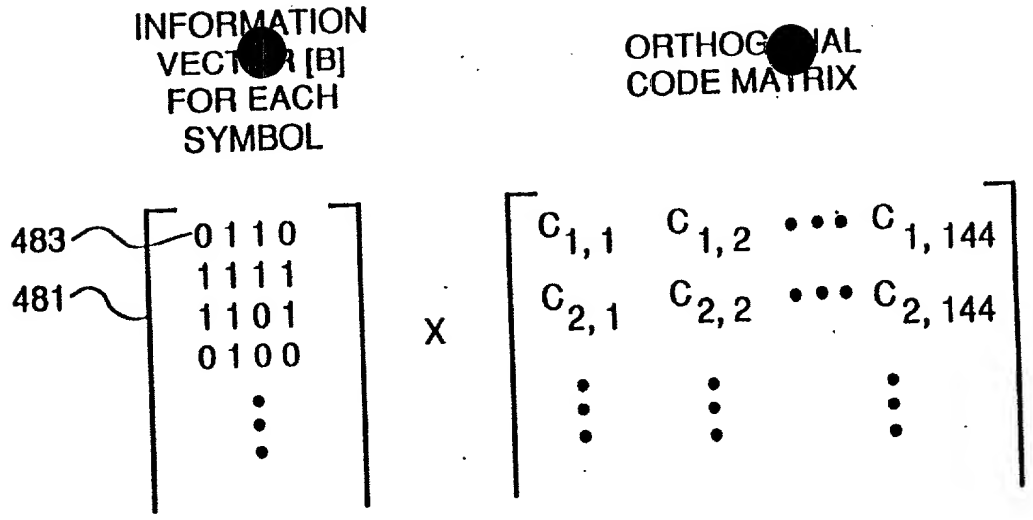
FIG. 21

CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 - j
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3* j
1001	101	011	= -3 + 3* j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
1100	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

403

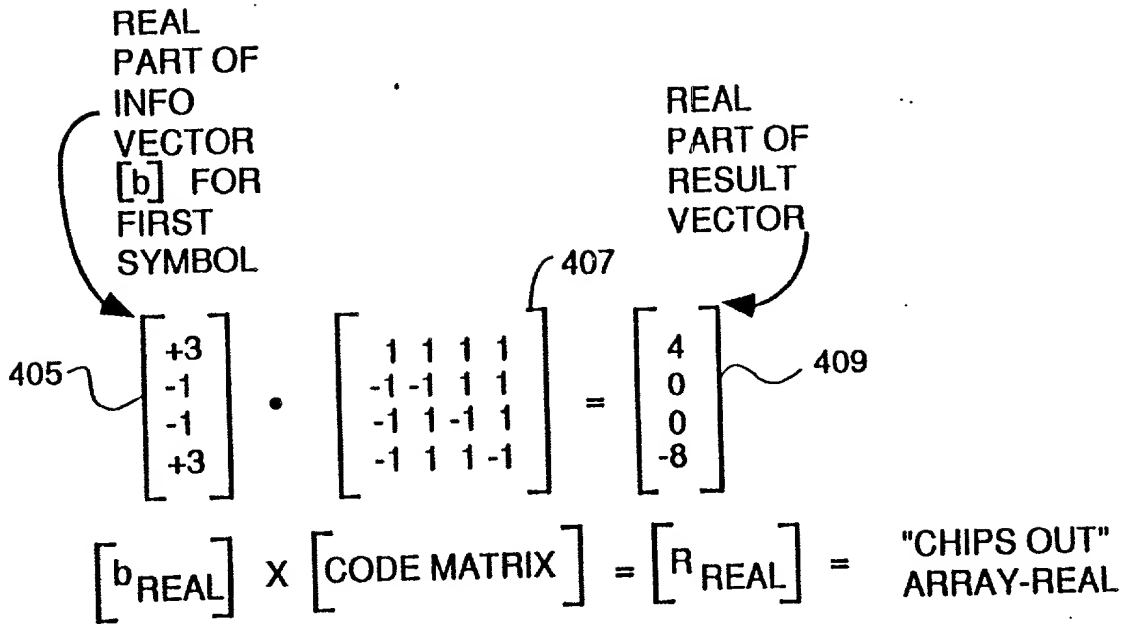
19

FIG. 22



20A

FIG. ~~23~~A



20B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

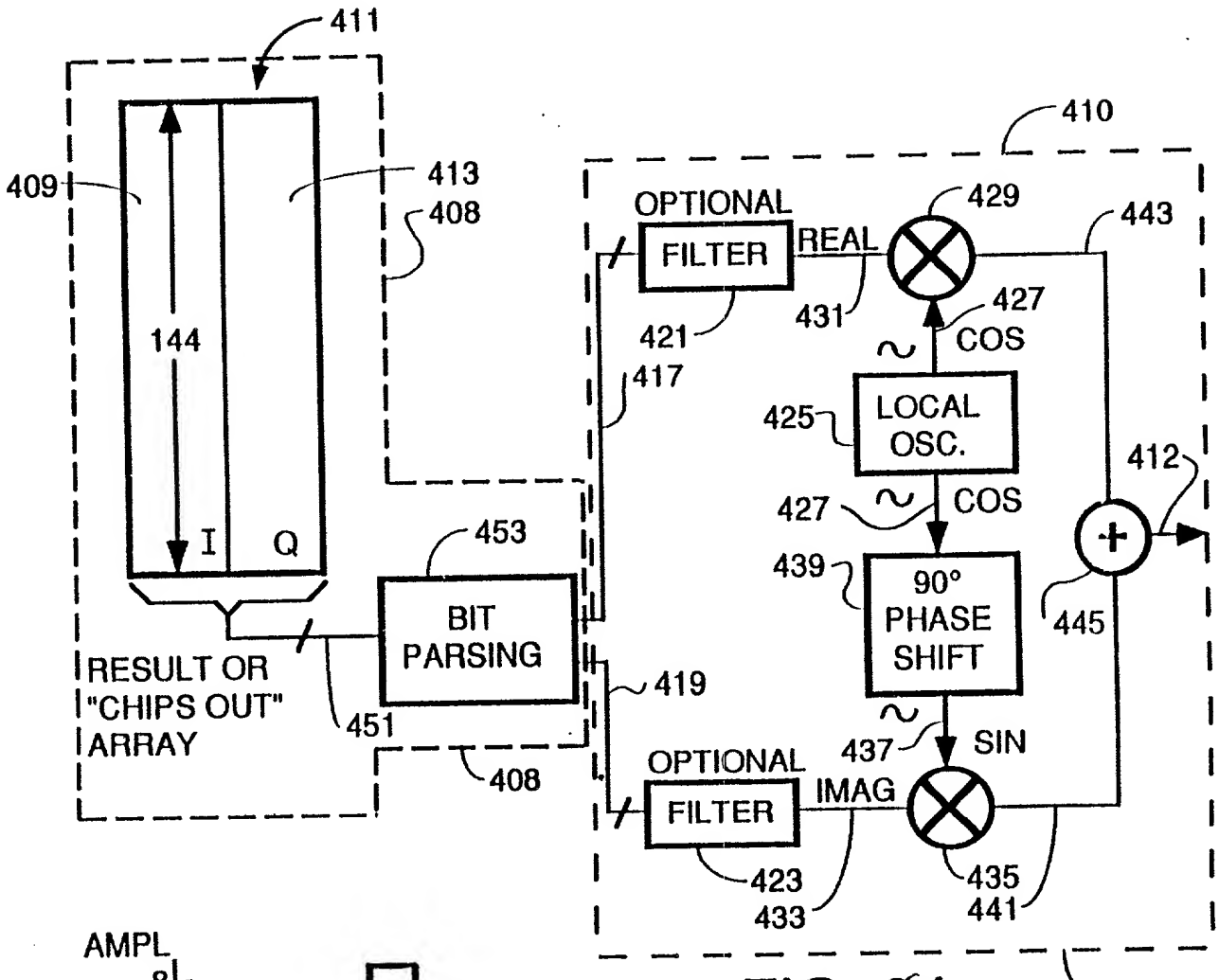

411
409
413
408
144
I
Q
453
BIT PARSING
RESULT OR "CHIPS OUT" ARRAY
451
408
410
OPTIONAL
FILTER
REAL
429
443
421
431
427
COS
417
425
LOCAL OSC.
412
427
COS
439
90° PHASE SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 24

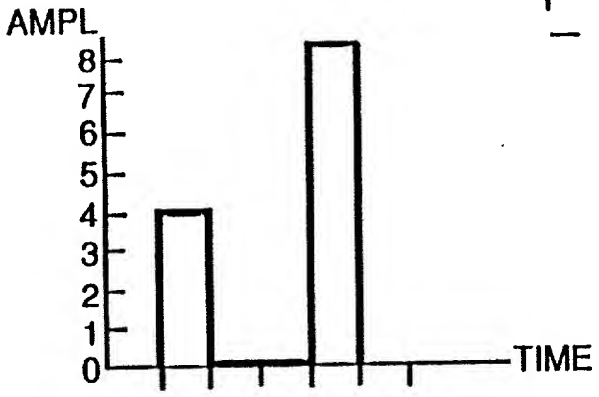
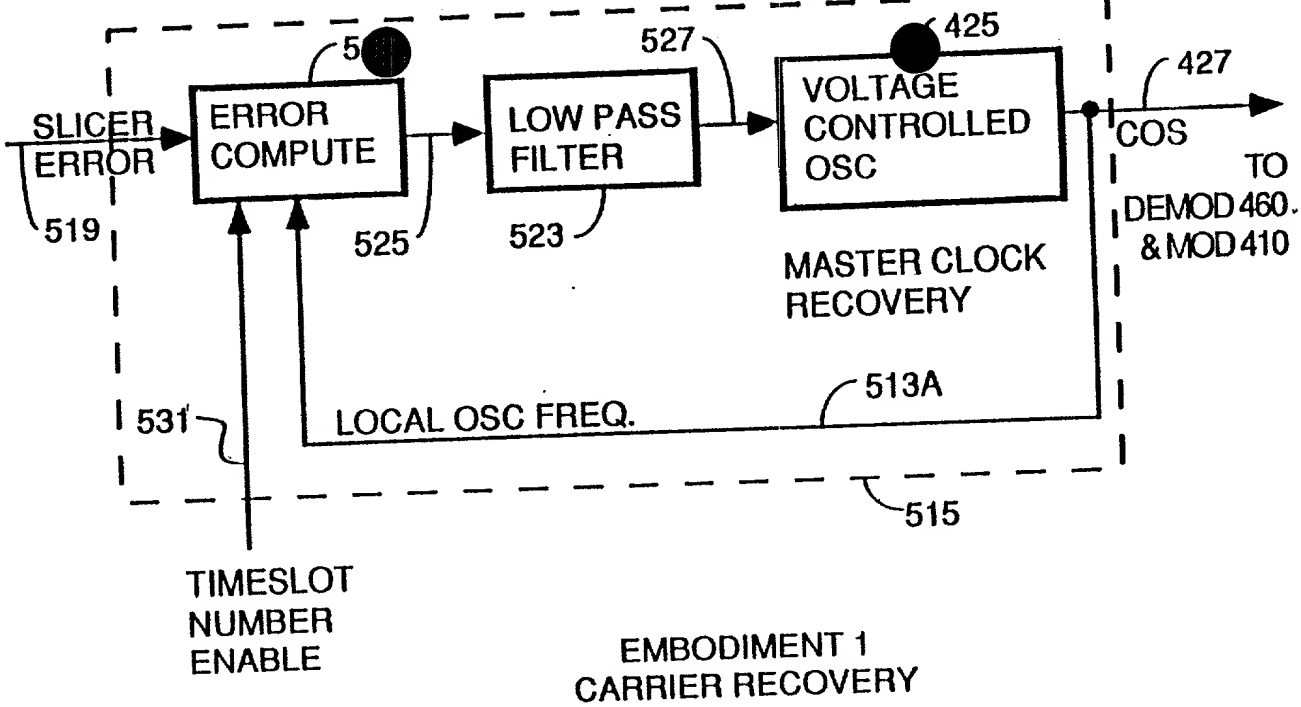

AMPL
8
7
6
5
4
3
2
1
0
TIME

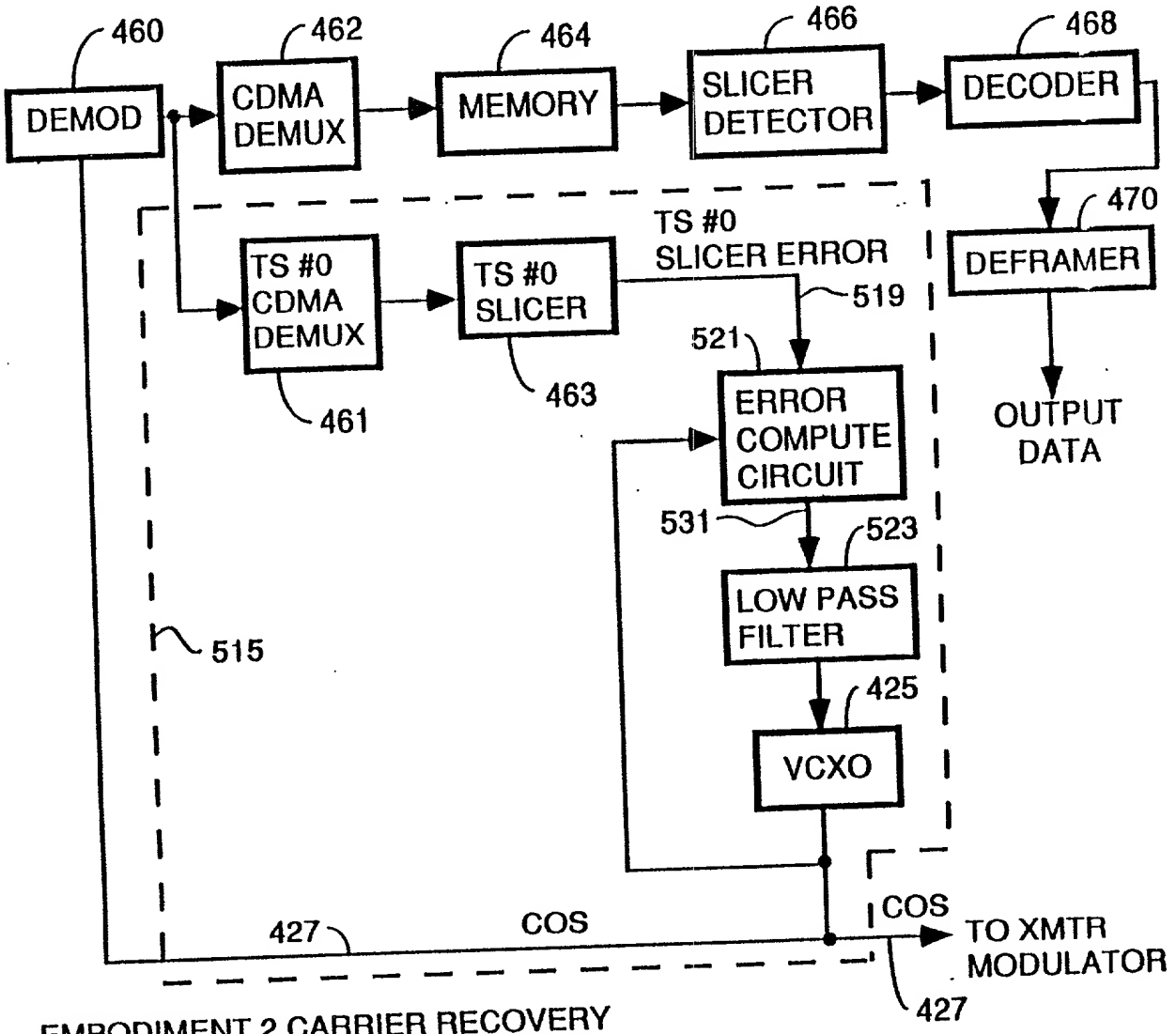
FIG. 25



EMBODIMENT 1
CARRIER RECOVERY

FIG. 35

25



EMBODIMENT 2 CARRIER RECOVERY

FIG. 36

26

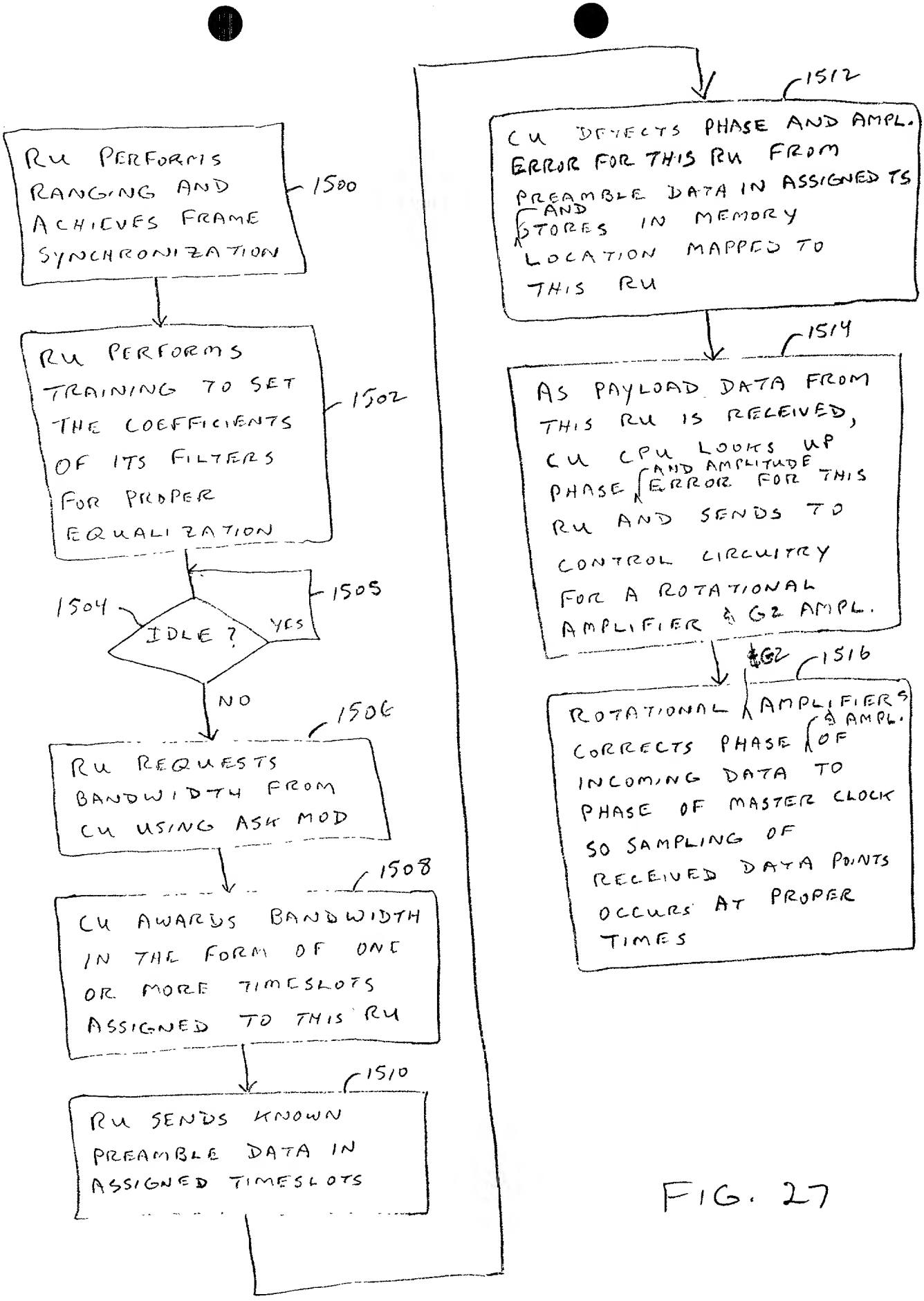
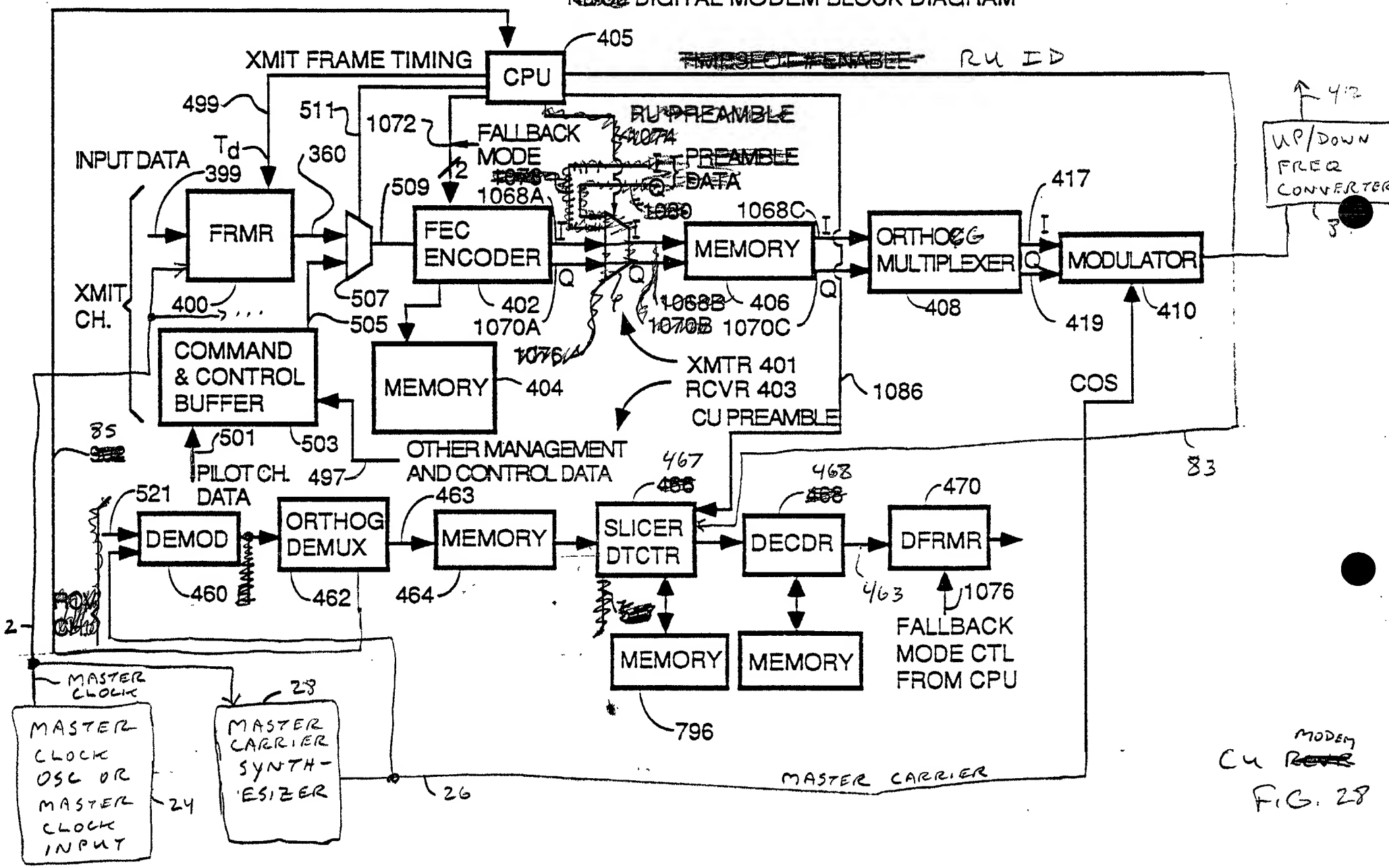

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1506
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1508
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1510
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1512
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1514
ROTATIONAL AMPLIFIERS & G2 AMPL. CORRECTS PHASE OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES
1516

FIG. 27

CU

DIGITAL MODEM BLOCK DIAGRAM



CU MODEM

FIG. 28

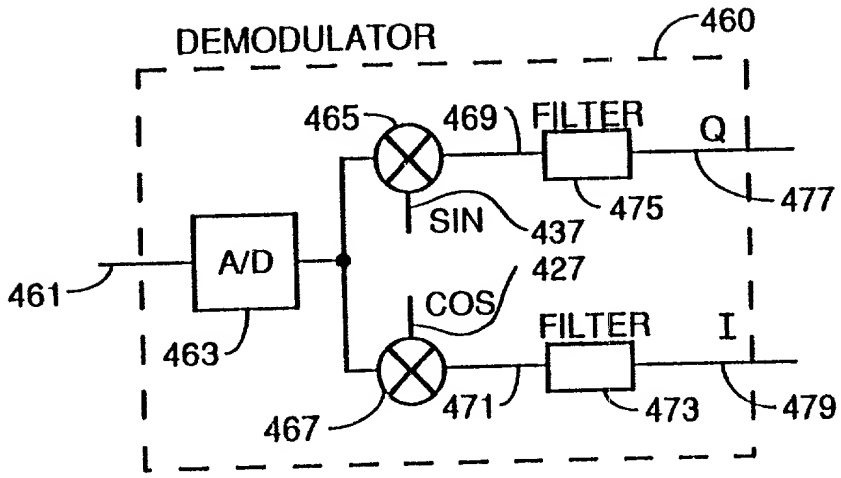

DEMODULATOR
460
465
469
FILTER
Q
475
477
SIN
437
461
A/D
427
COS
FILTER
I
463
467
471
473
479

FIG. 29

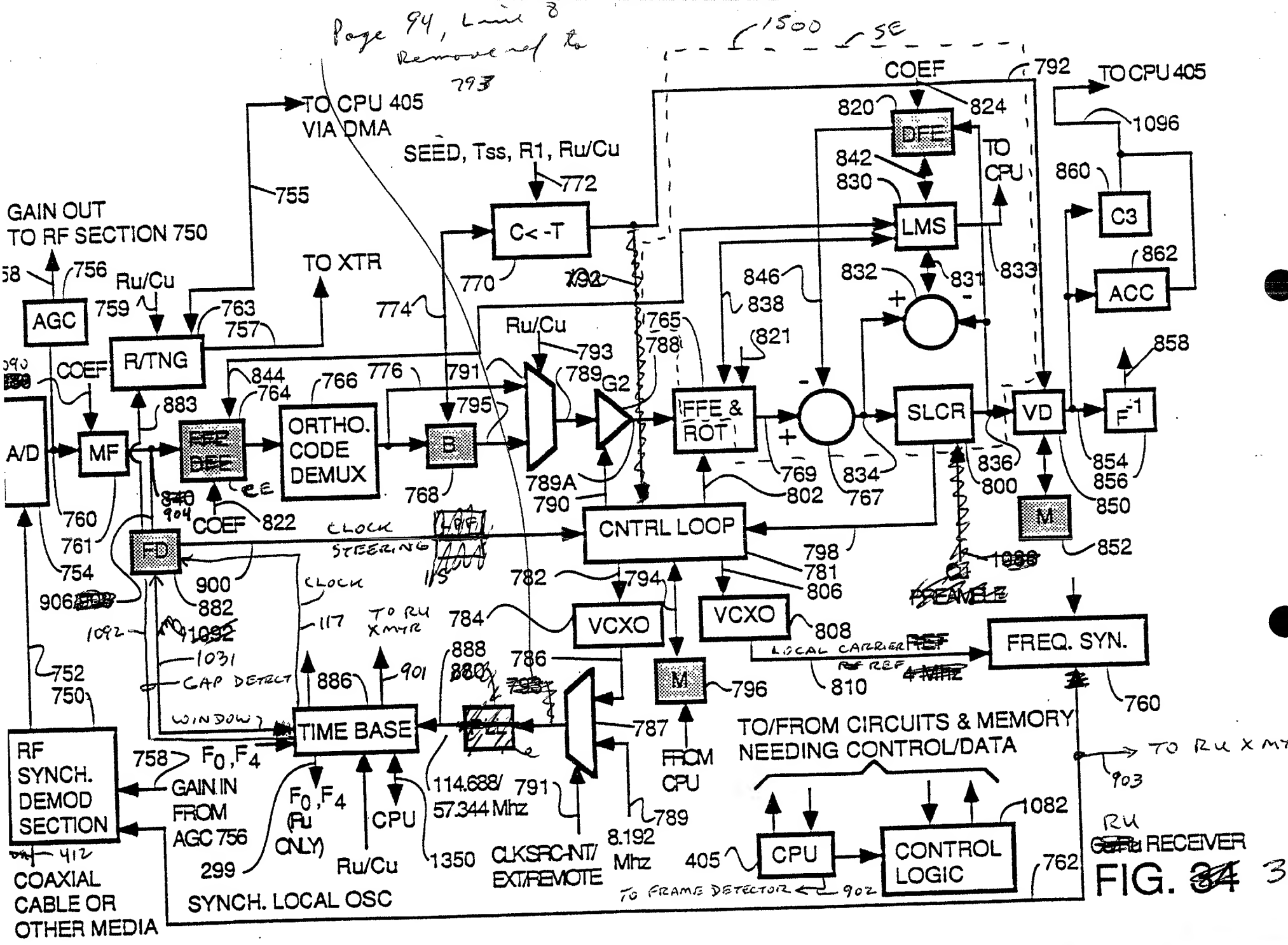


FIG. 84 30

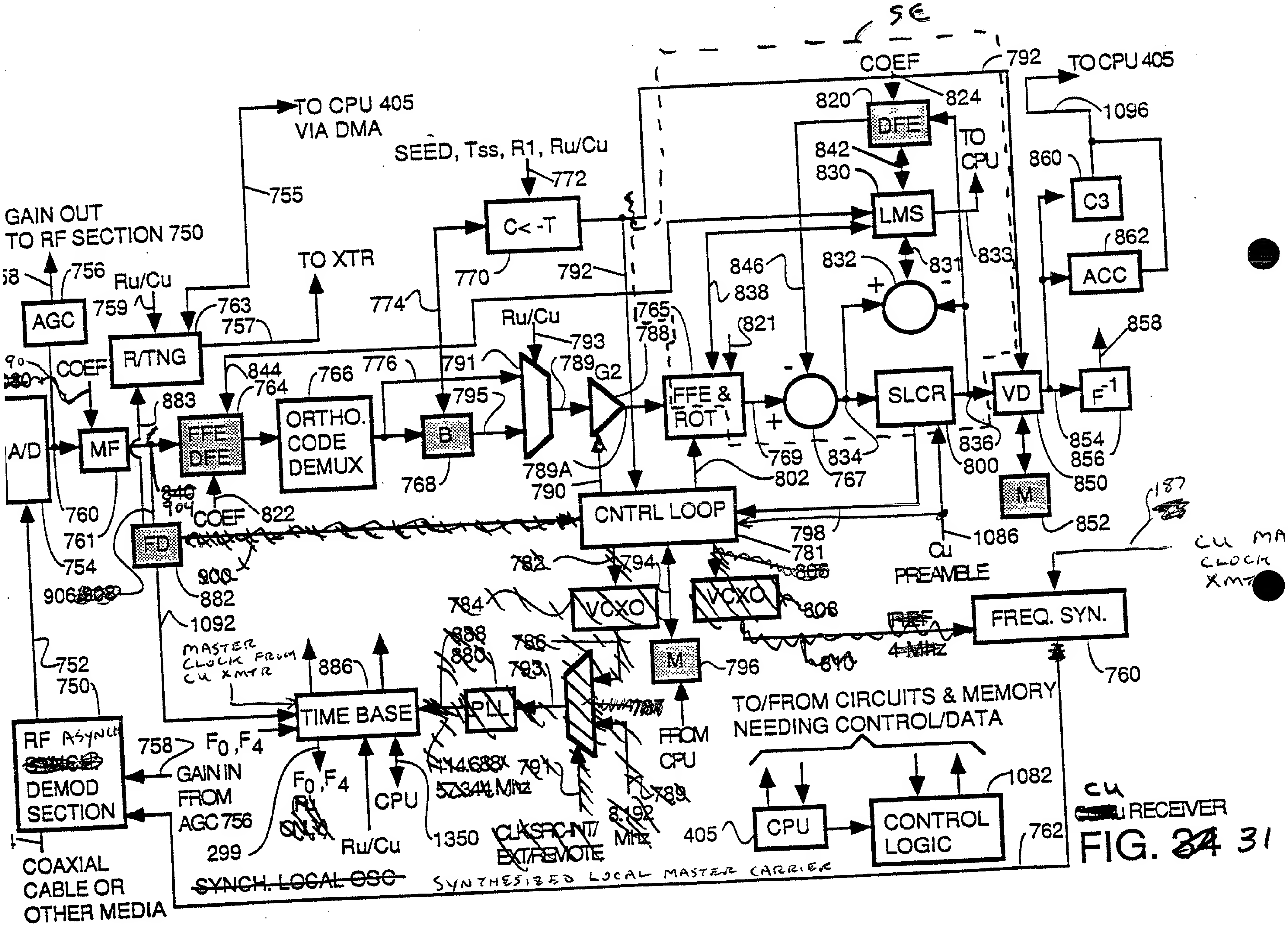
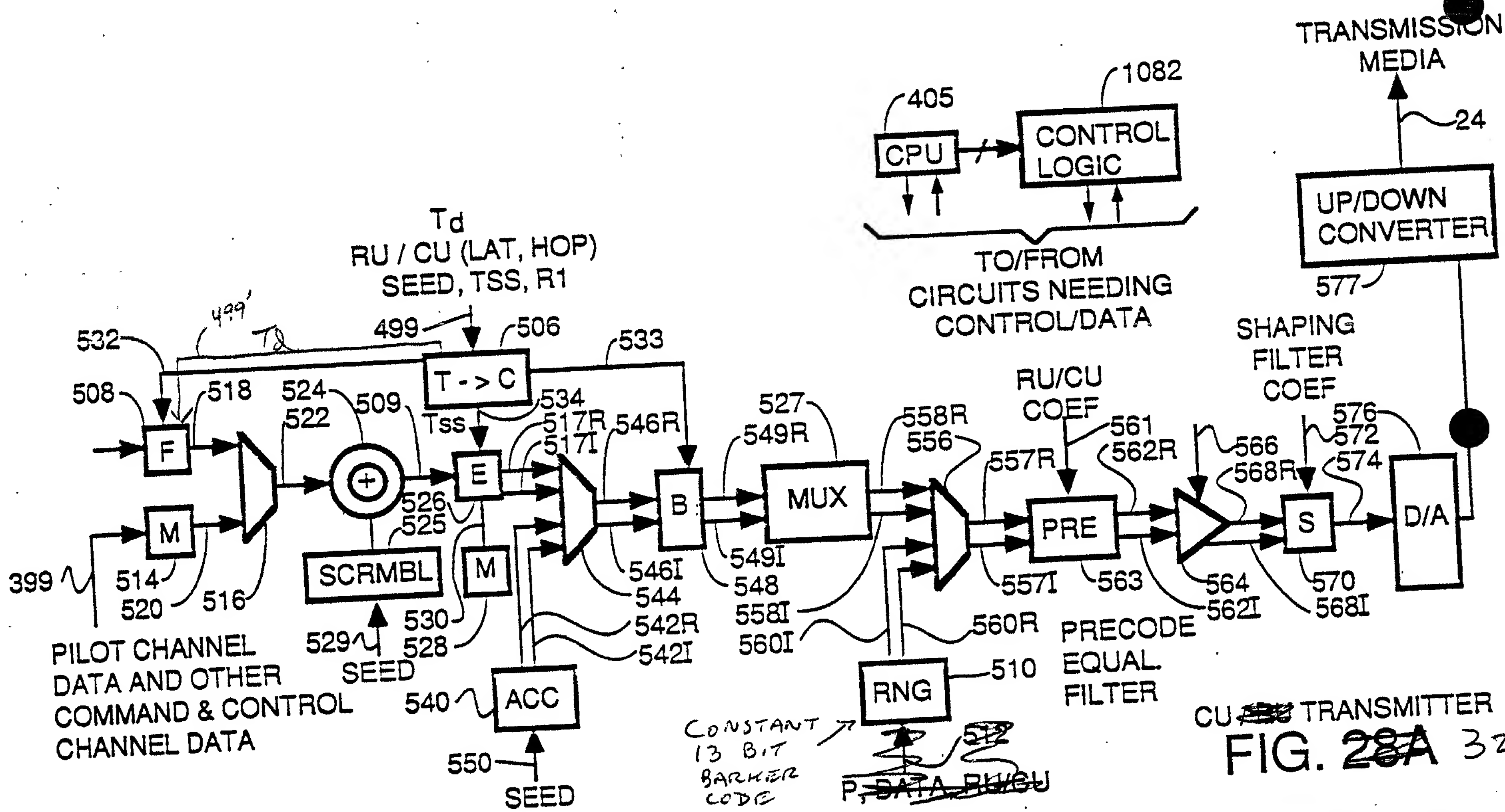

TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
GAIN OUT
TO RF SECTION 750
TO XTR
TO CPU 405
COEF
SE
AGC
R/TNG
MF
A/D
FFE DFE
ORTHO. CODE DEMUX
B
C< -T
G2
FFE & ROT
SLCR
LMS
DFE
TO CPU
VD
F^{-1}
C3
ACC
M
CNTRL LOOP
FD
VCXO
VCXO
M
FREQ. SYN.
PREAMBLE
Cu
TIME BASE
PLL
FROM CPU
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
CPU
CONTROL LOGIC
RF ASYNCH DEMOD SECTION
GAIN IN FROM AGC 756
F_0, F_4
CPU
Ru/Cu
CLKSRC INT/EXT/REMOTE
8.192 MHz
MASTER CLOCK FROM CU XMTR
CU MASTER CLOCK XMTR
SYNCH. LOCAL OSC
SYNTHESIZED LOCAL MASTER CARRIER
COAXIAL CABLE OR OTHER MEDIA
CU RECEIVER

FIG. 31



CU TRANSMITTER

FIG. 28A 32

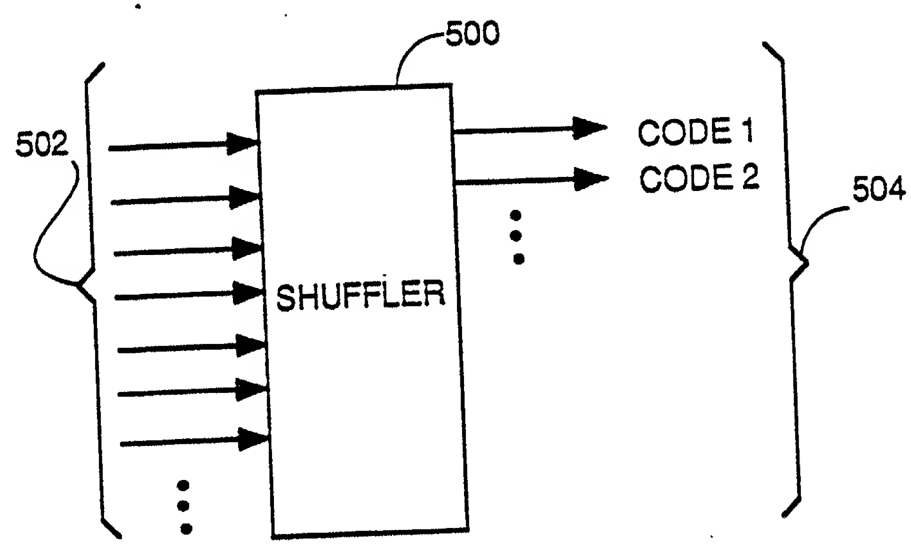
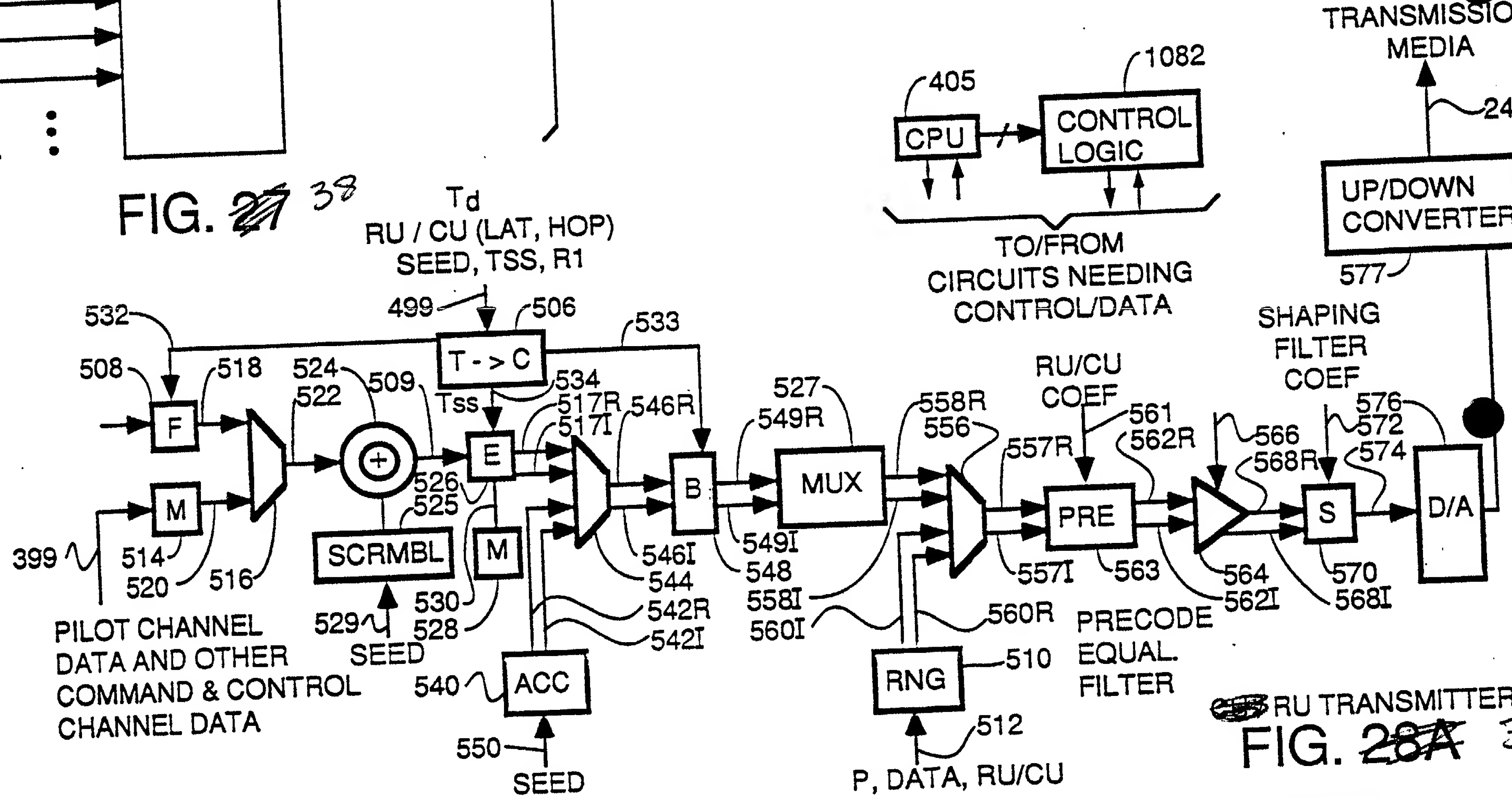
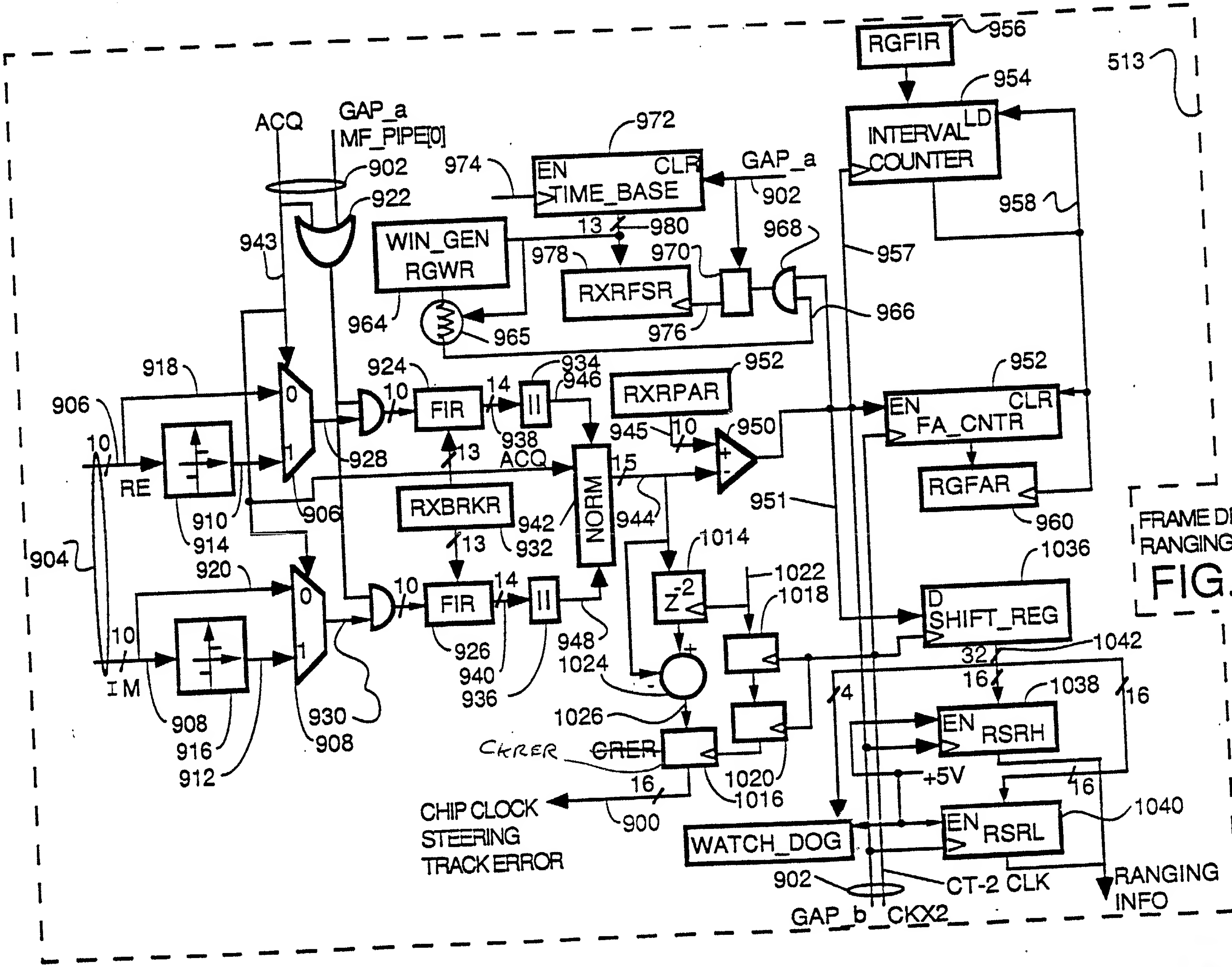


FIG. 38



RU TRANSMITTER

FIG. 39



FRAME DETECTOR/
RANGING DETECTO
513
RGFIR
956
954
INTERVAL
LD
COUNTER
958
957
ACQ
GAP_a
MF_PIPE[0]
902
922
943
974
972
EN
CLR
TIME_BASE
GAP_a
902
13
980
WIN_GEN
RGWR
978
970
968
RXRFSR
966
964
965
976
952
EN
FA_CNTR
CLR
RGFAR
960
918
906
RE
IM
10
904
910
914
920
924
FIR
14
934
946
RXRPAR
945
950
938
ACQ
928
13
NORM
15
951
RXBRKR
942
932
944
1014
z^-2
1022
1018
D
SHIFT_REG
1036
1042
32
16
1038
EN
RSRH
+5V
EN
RSRL
1040
4
WATCH_DOG
CT-2 CLK
RANGING
INFO
GAP_b
CKX2
926
940
936
948
1024
1026
930
908
916
912
Ckrer
GRER
1020
1016
900
CHIP CLOCK
STEERING
TRACK ERROR

FIG. ~~38~~

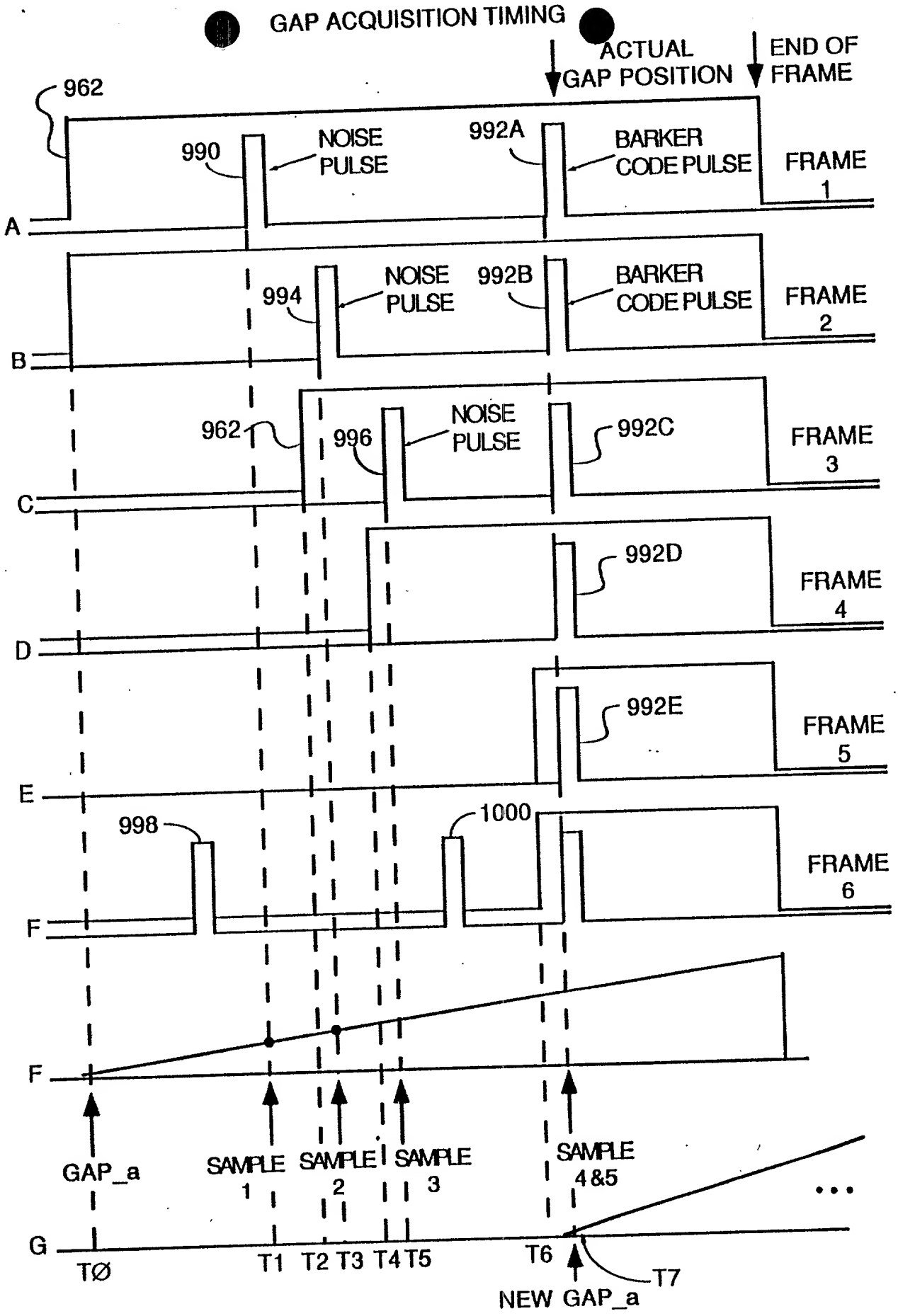
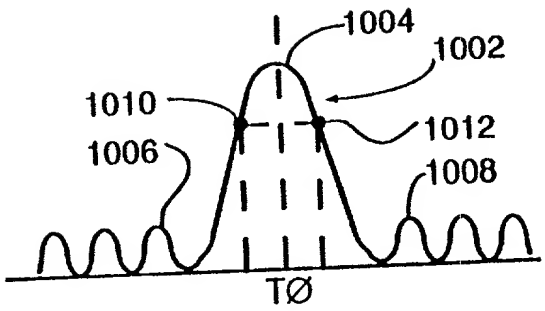
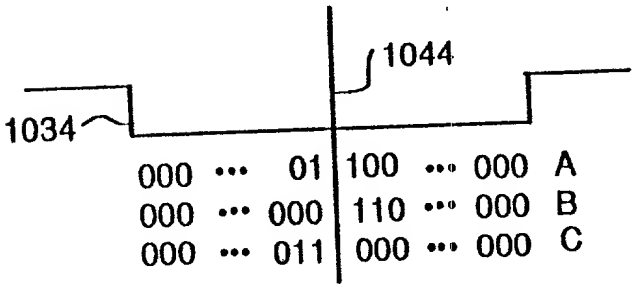

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
...
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 39 35



36

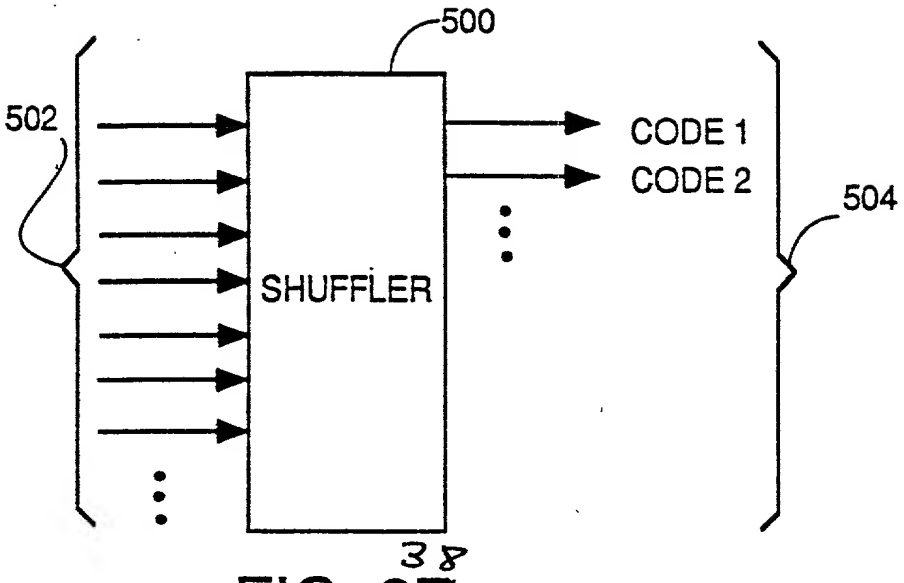
FIG. ~~40~~



37

FIG. ~~41~~

FINE TUNING TO CENTER BARKER CODE



38

FIG. 27

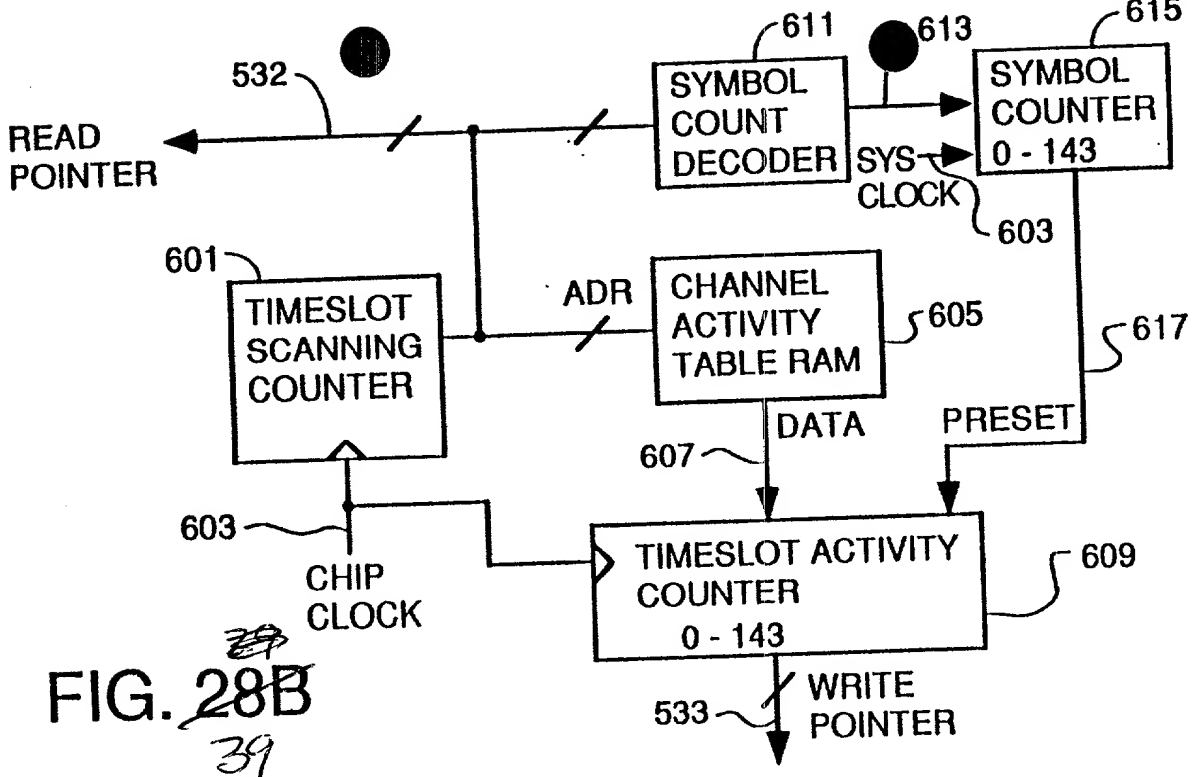


FIG. 28B

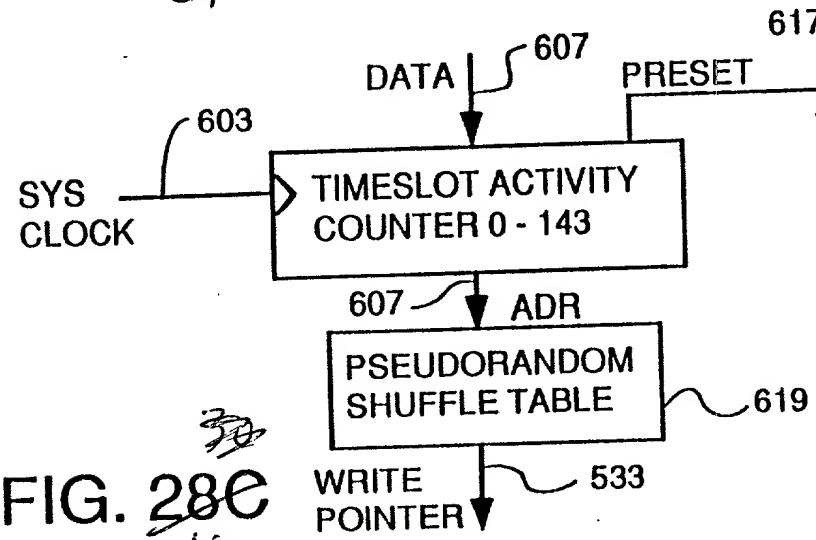


FIG. 28C

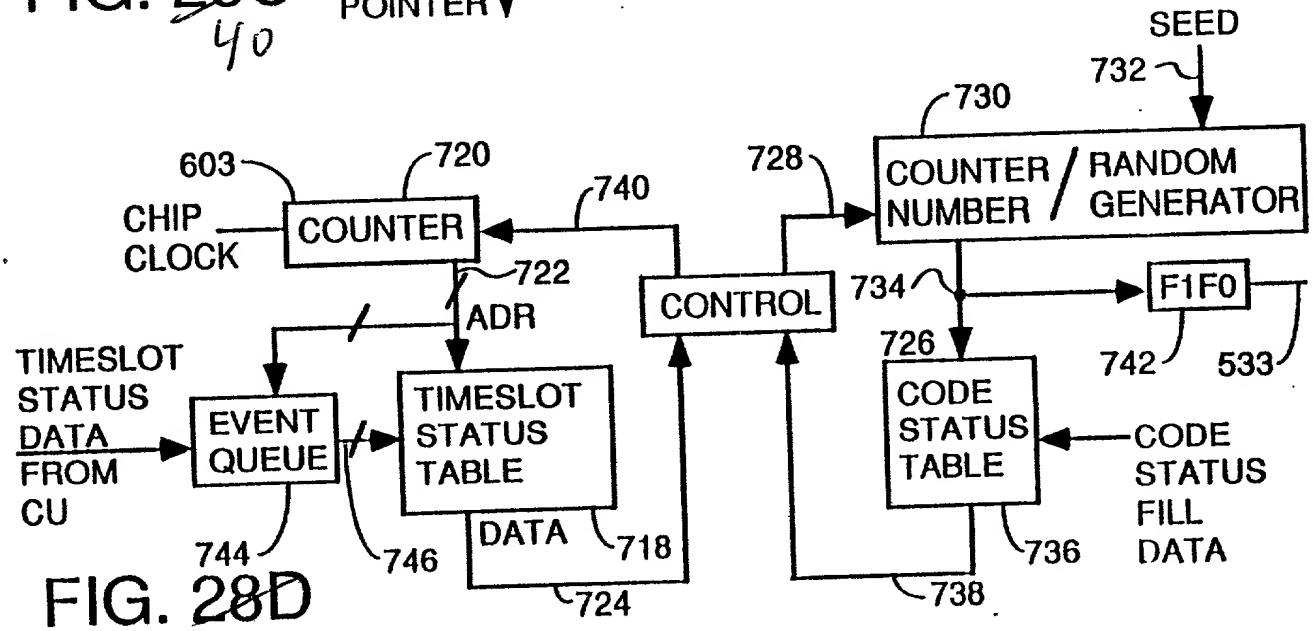
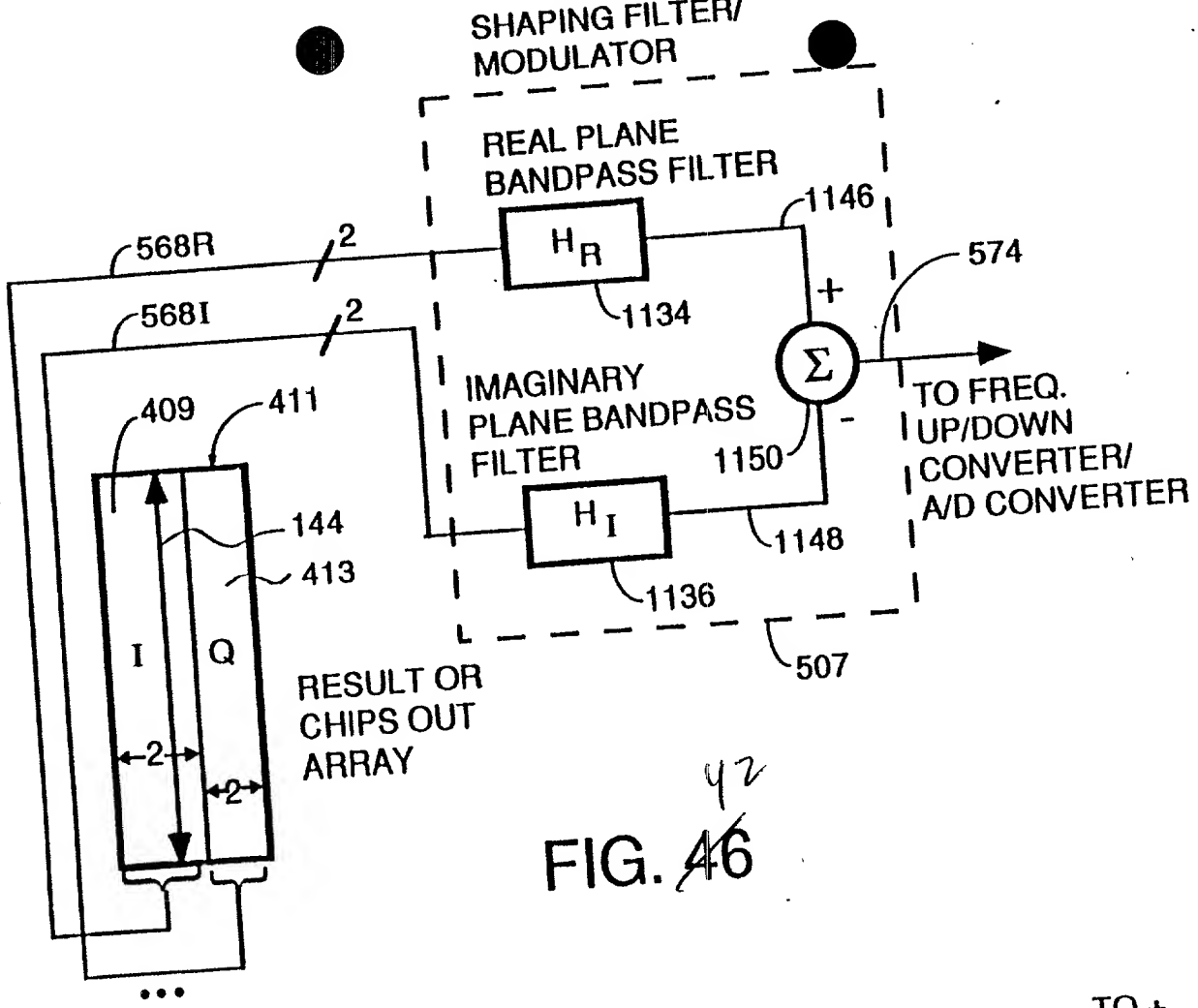
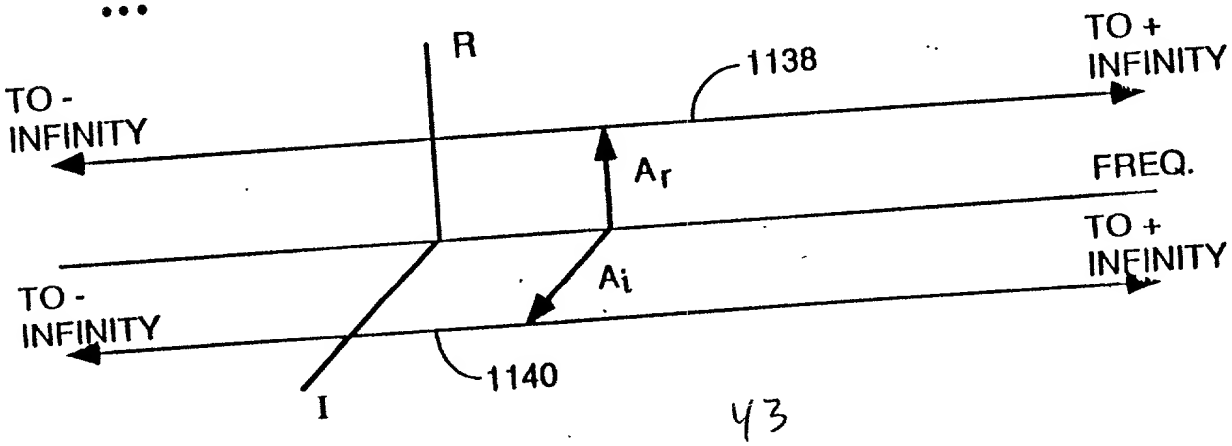


FIG. 28D



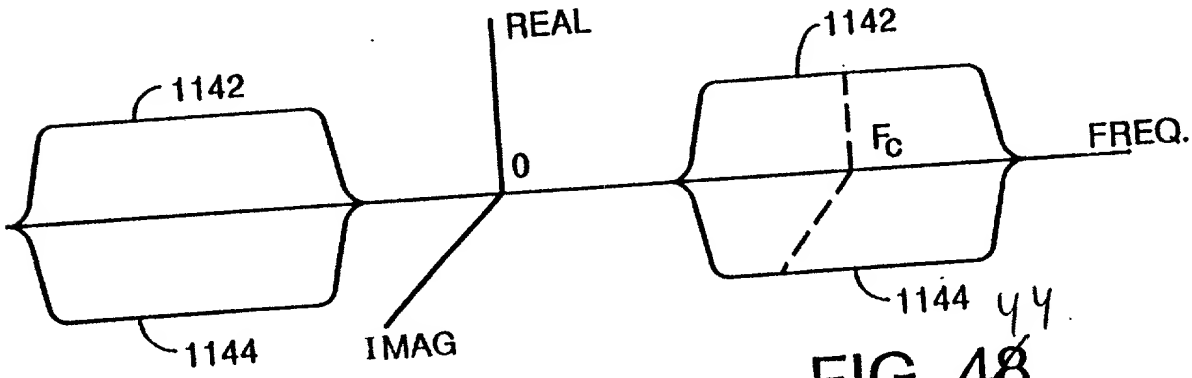
42

FIG. 46



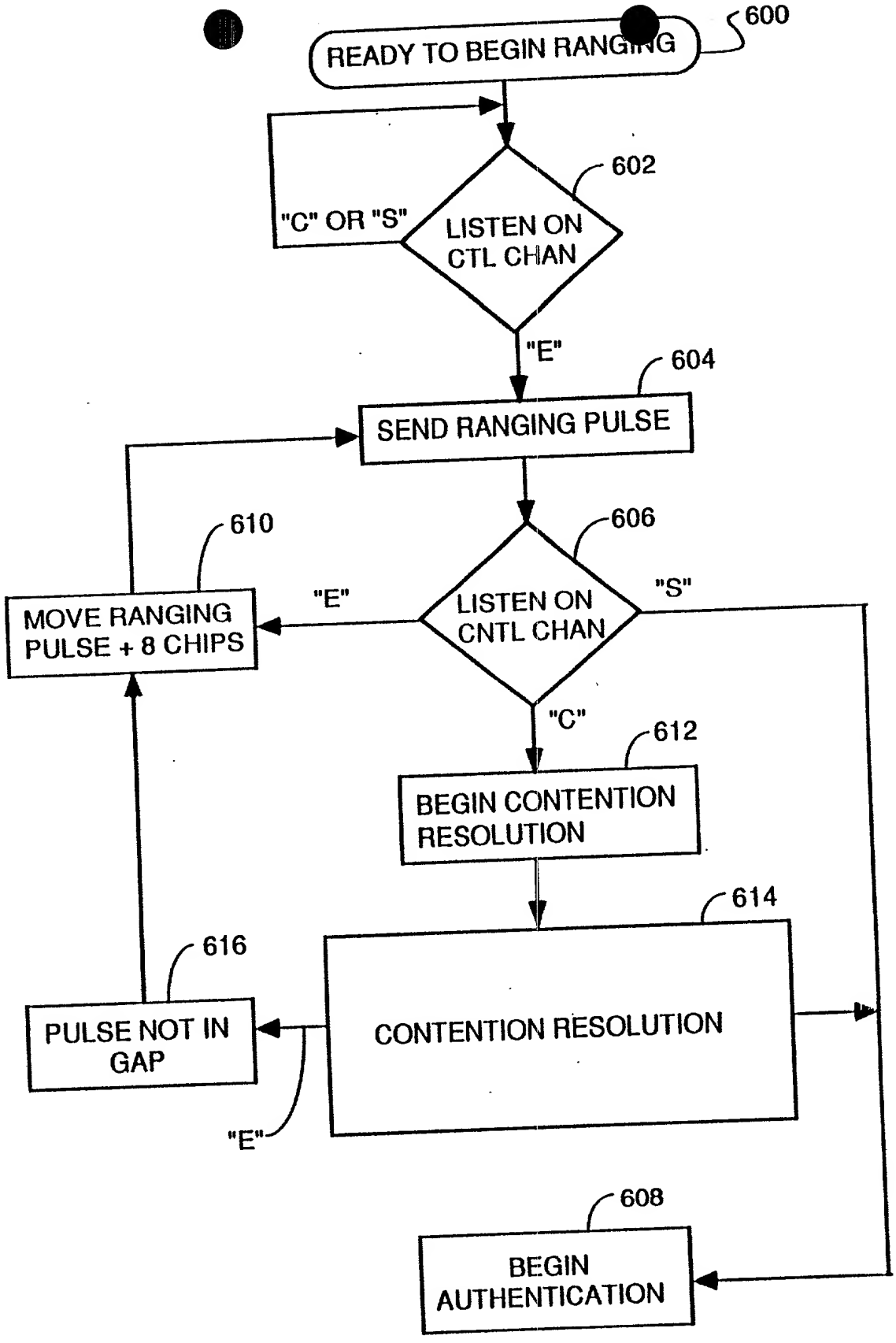
43

FIG. 47



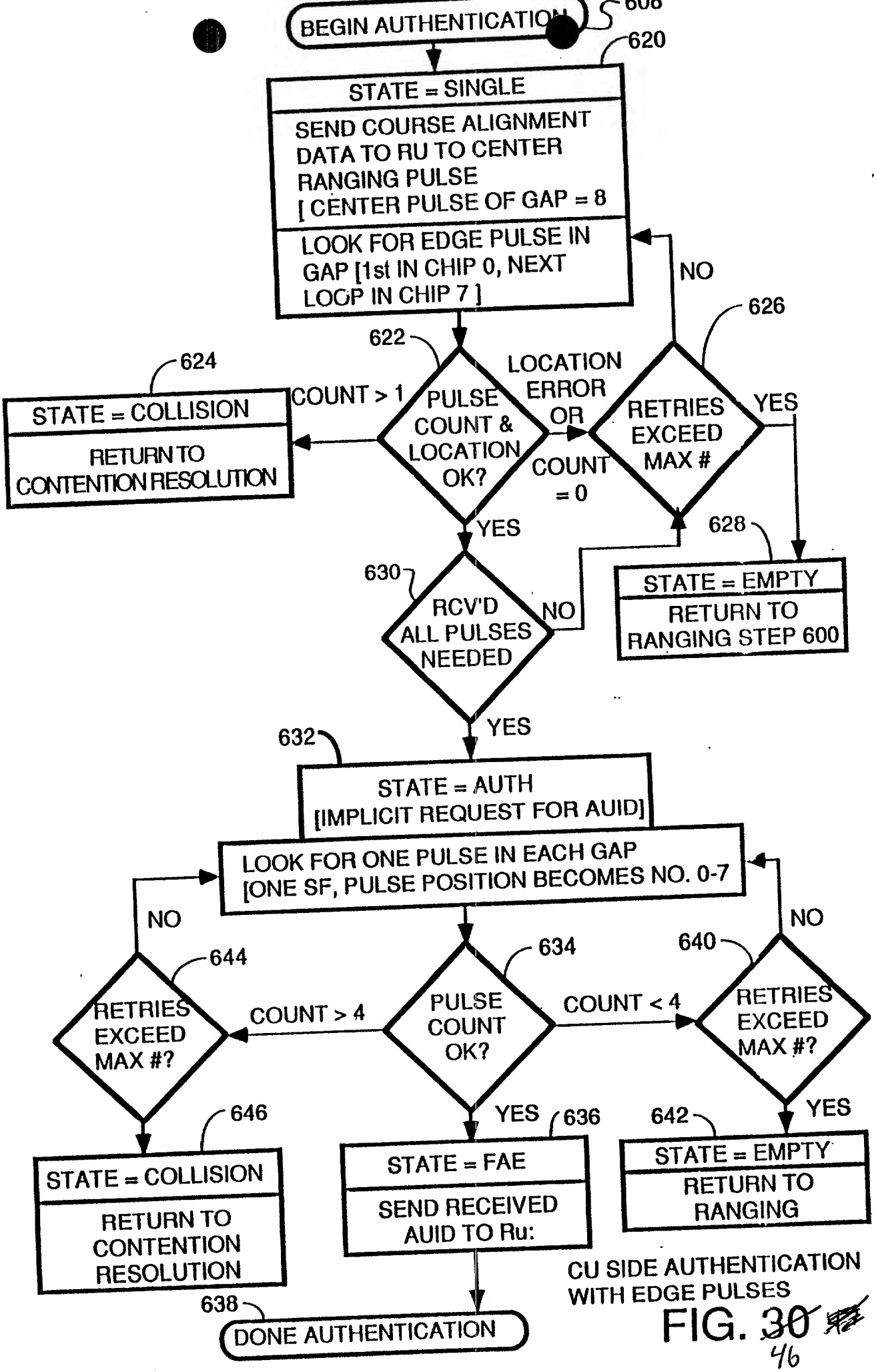
44

FIG. 48



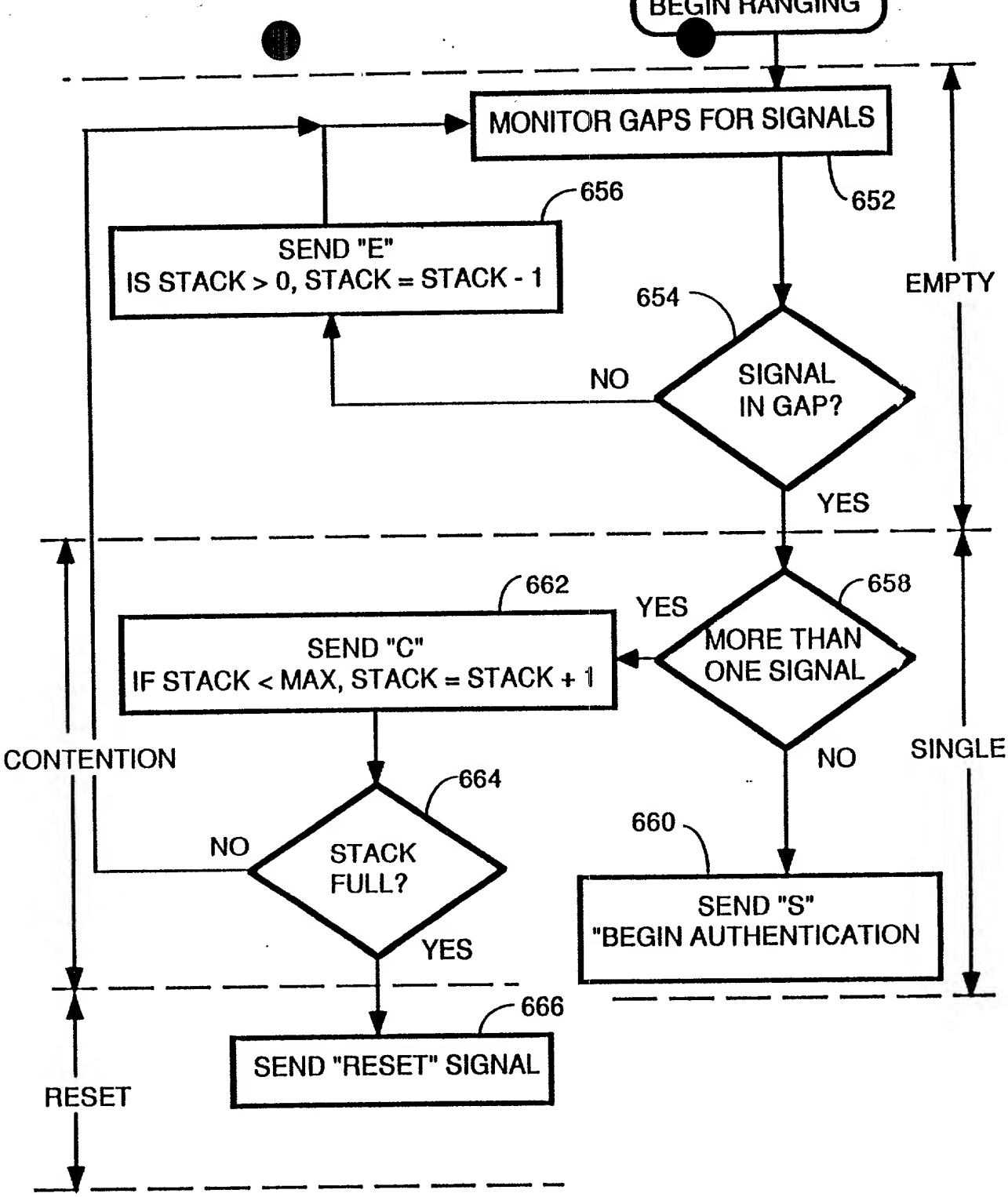
RU RANGING

FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30

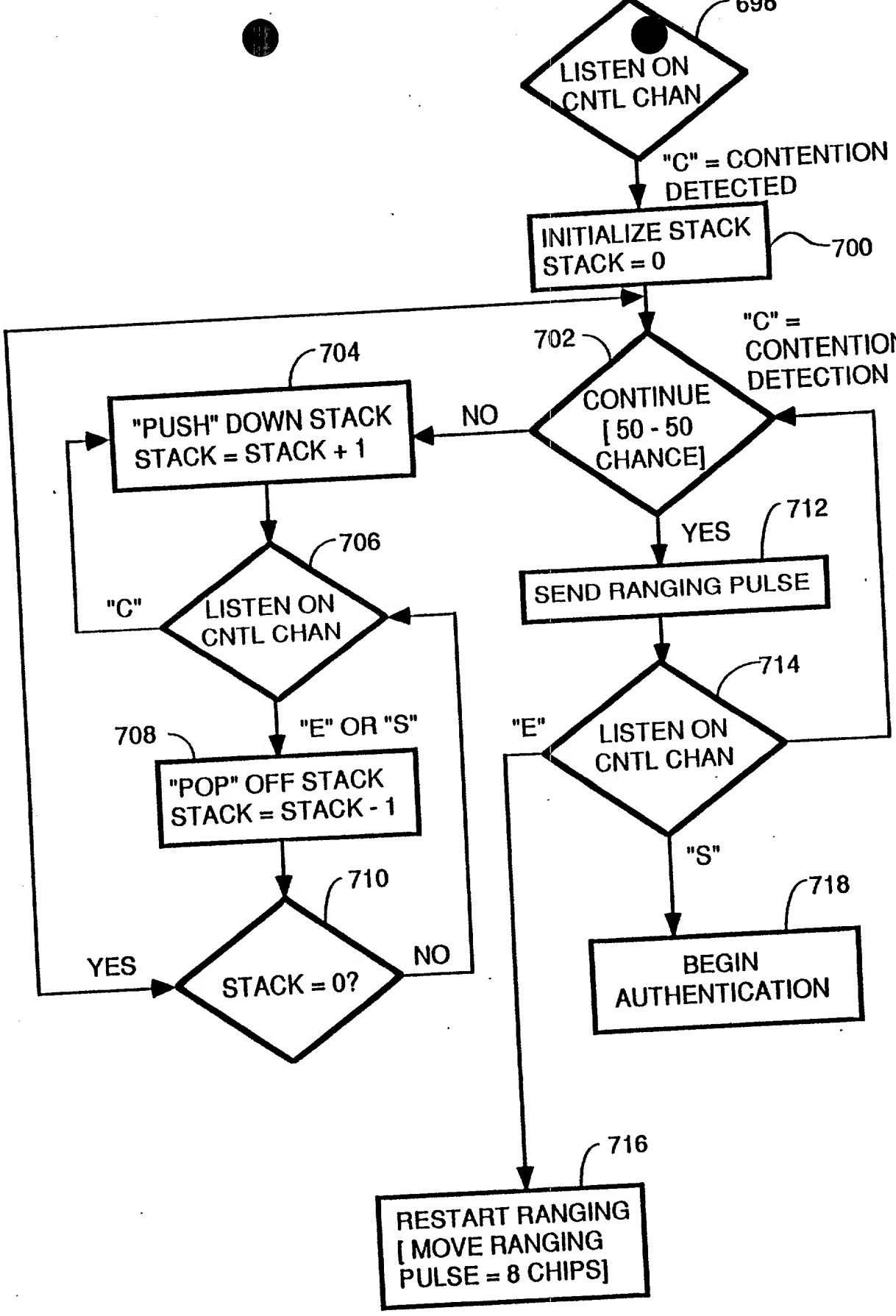


CU RANGING & CONTENTION RESOLUTION

~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

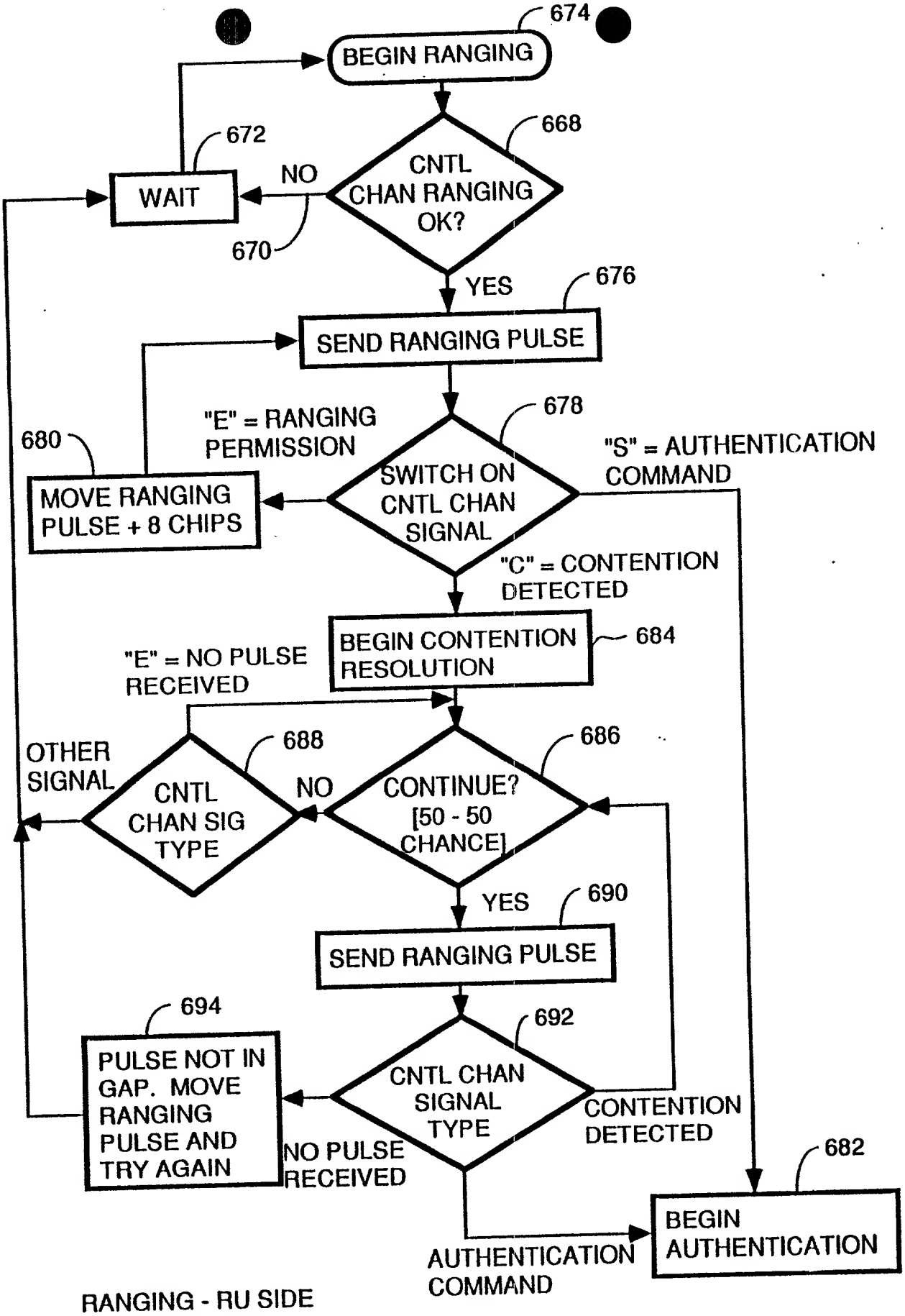
FIG. 31 48

47



CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. 33



RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. 32

50
49

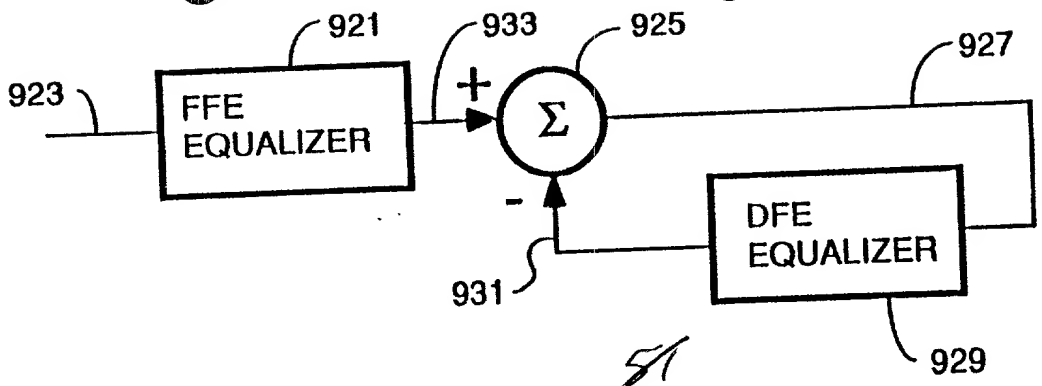


FIG. 37

50

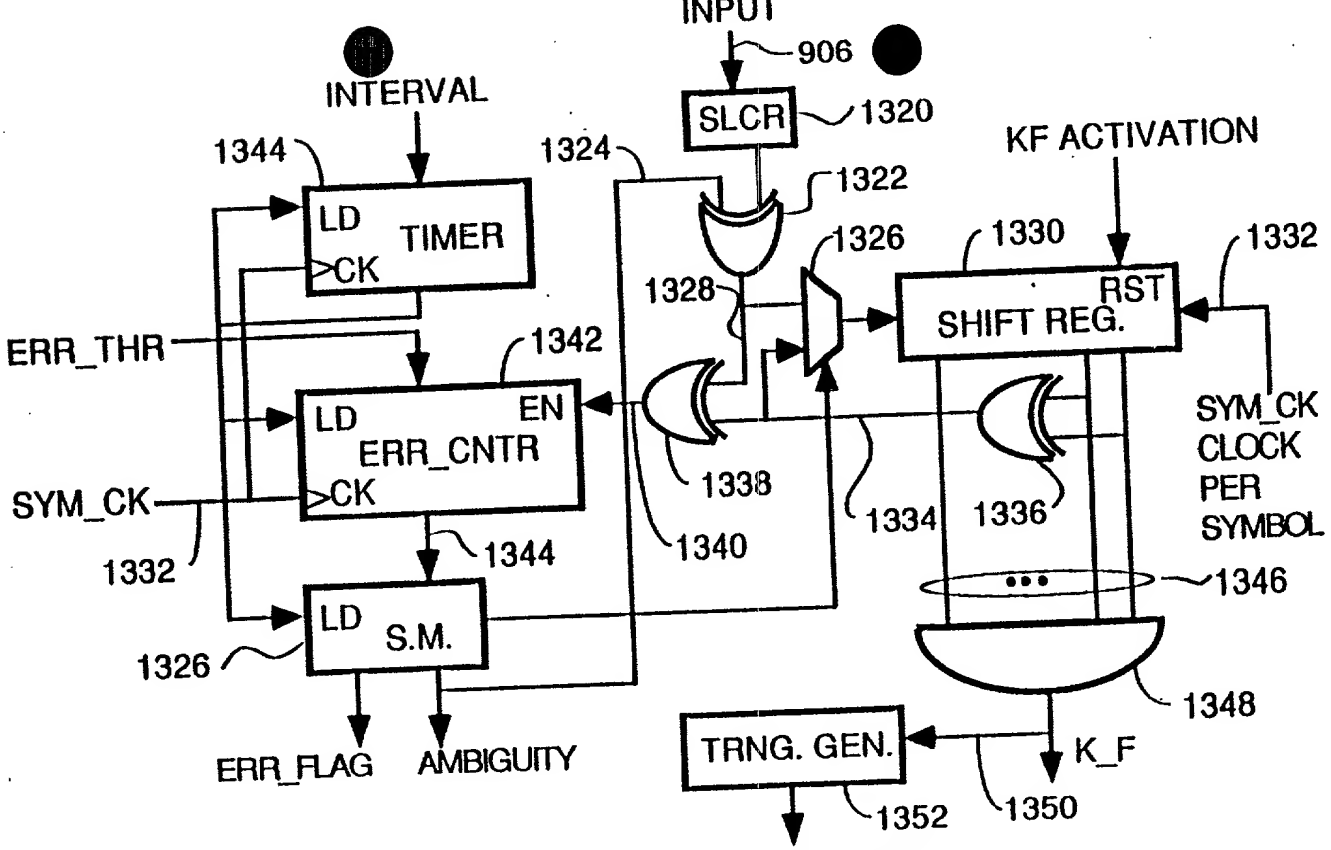
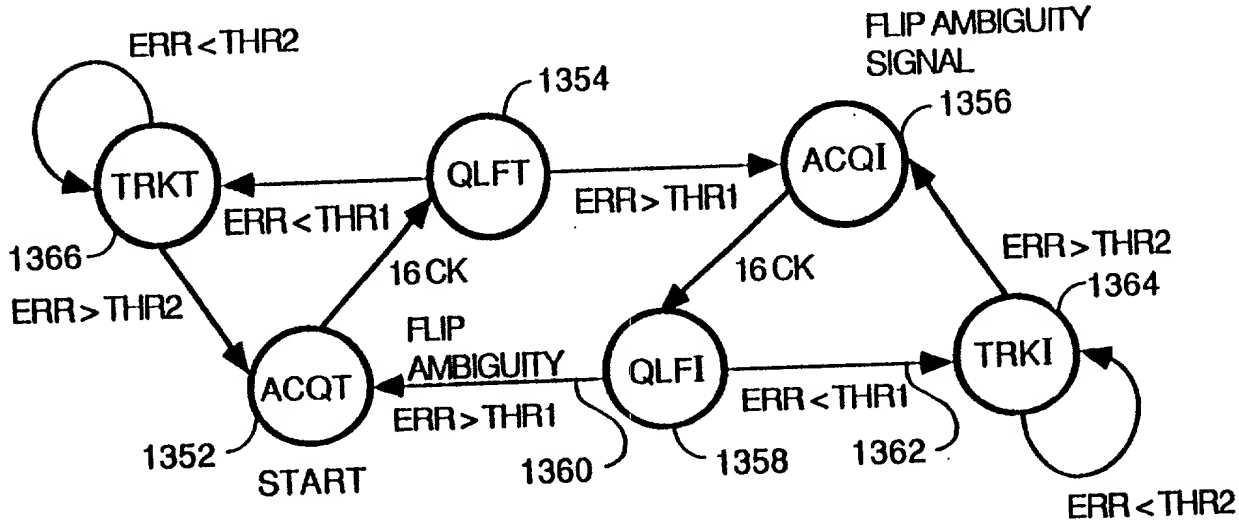


FIG. 52

51



STATE MACHINE

FIG. 53

52

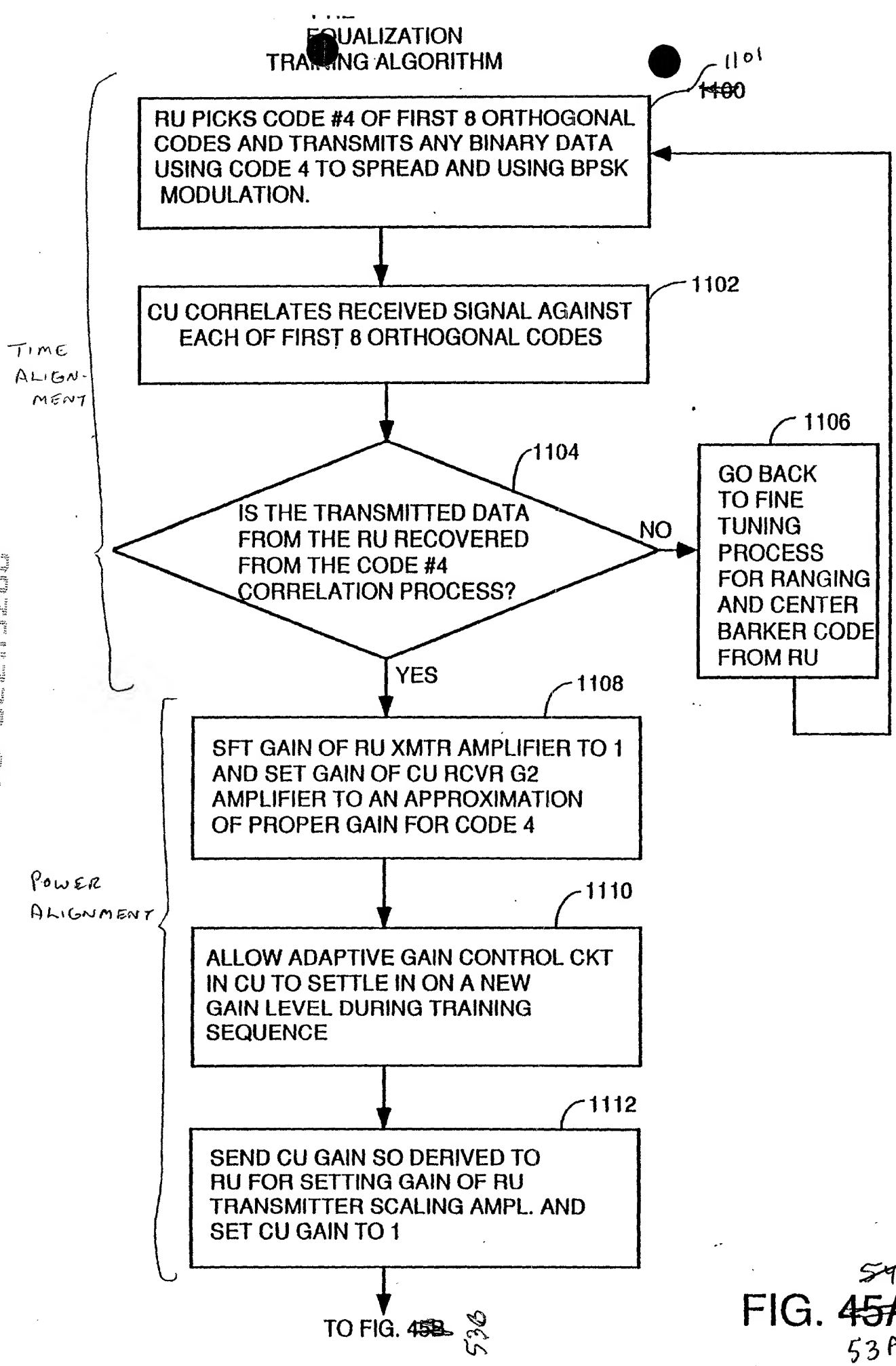


FIG. 45A
54A
53A

UPSTREAM EQUALIZATION

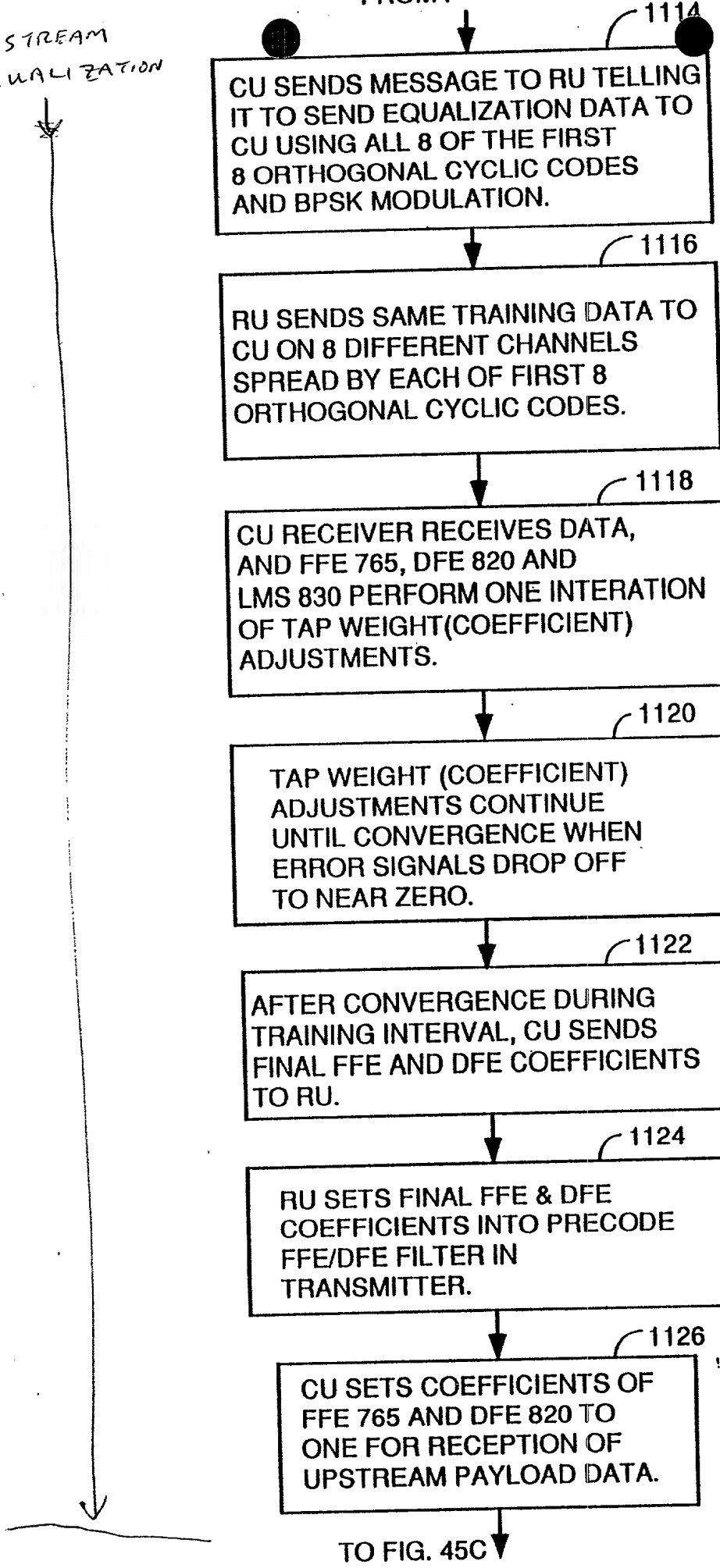


FIG. ~~45B~~ 54B
53B

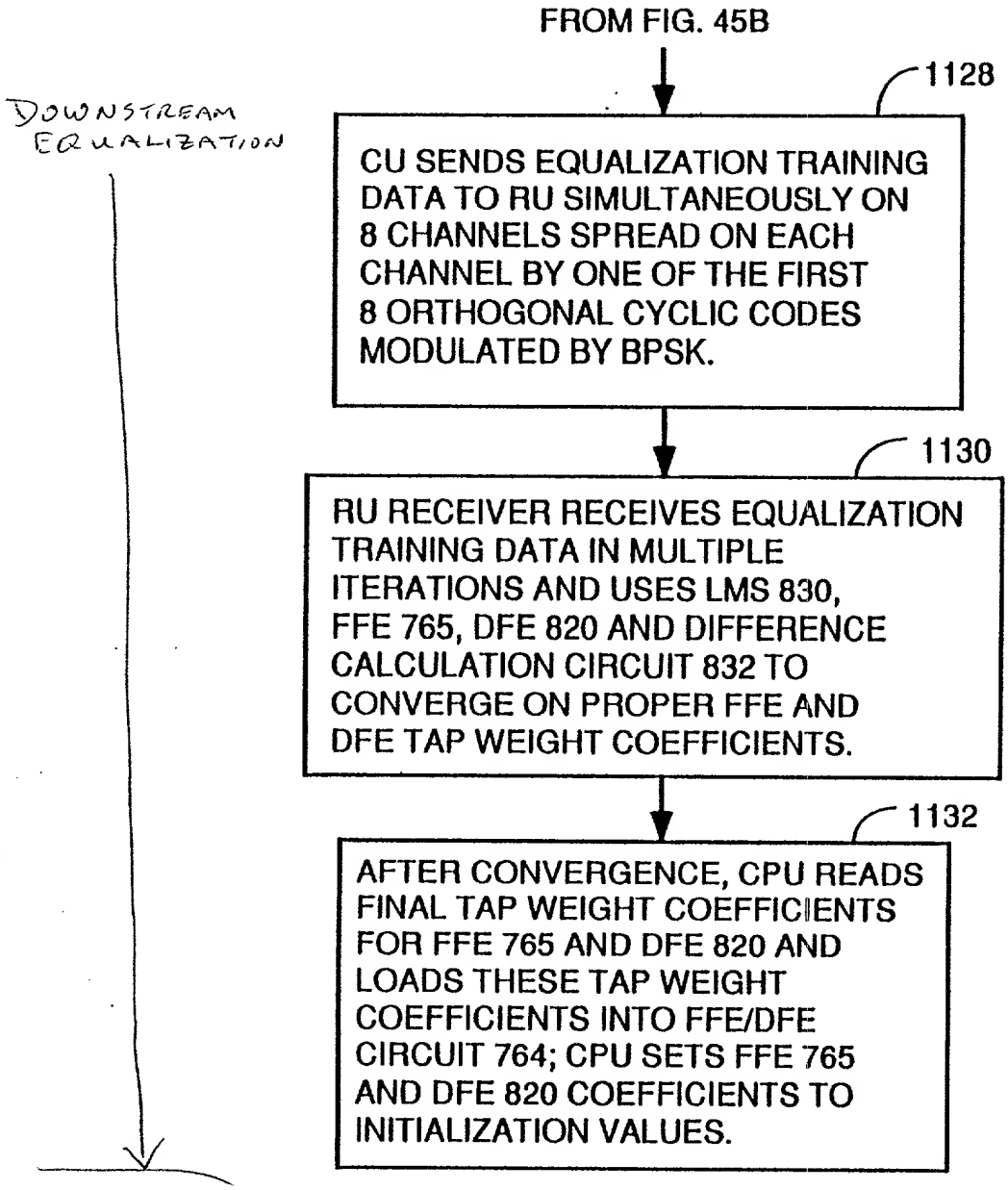


FIG. ~~45C~~ 54C 53C

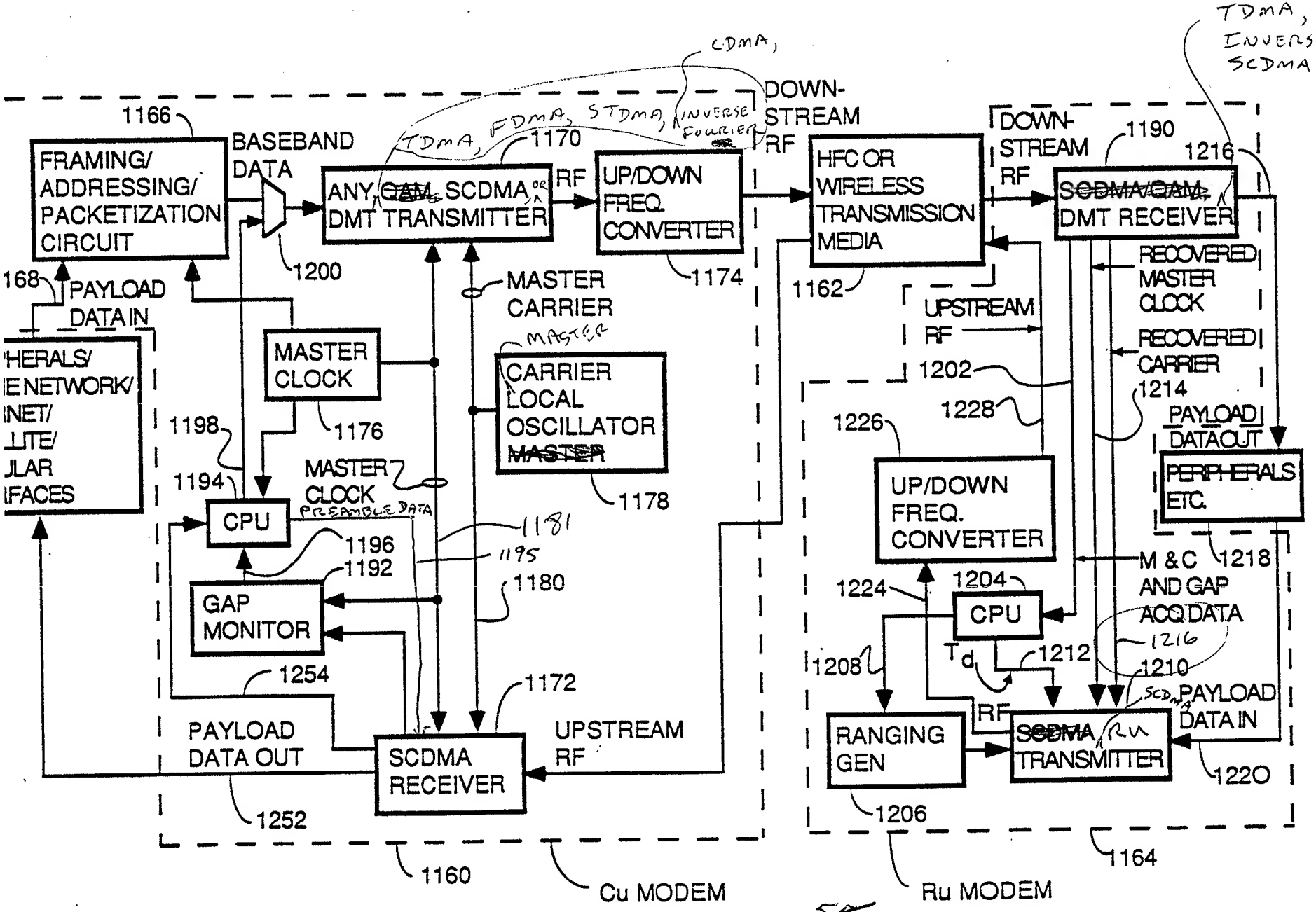
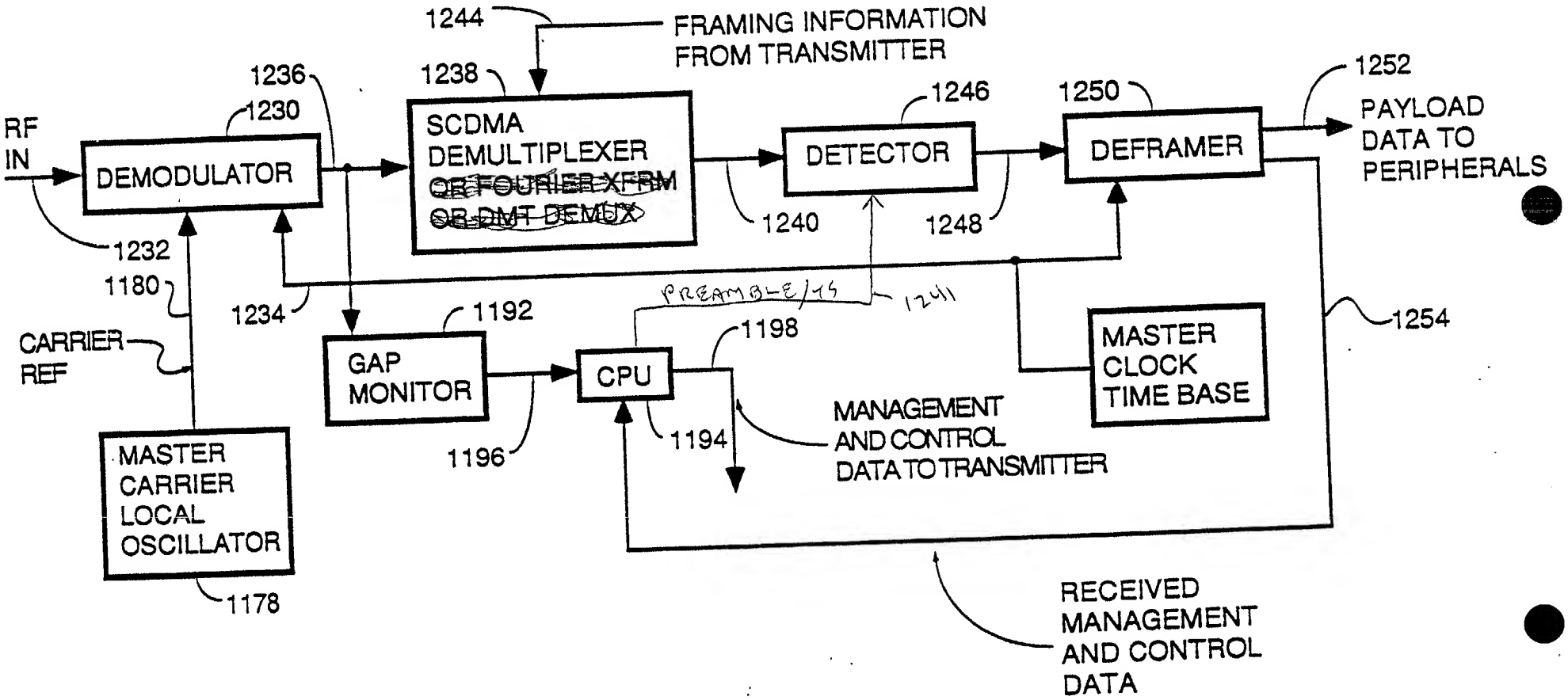


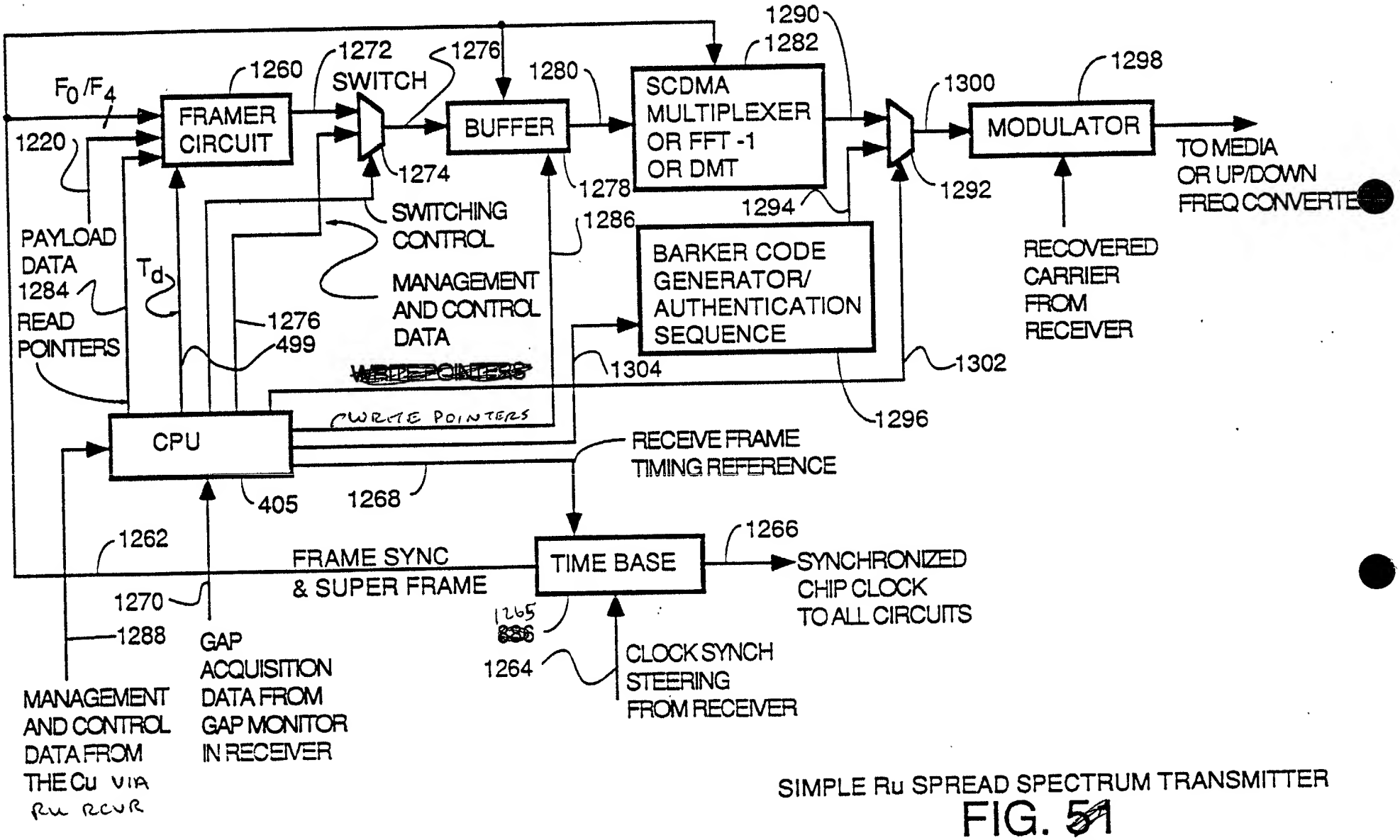
FIG. ~~49~~ 54



SIMPLE Cu SPREAD SPECTRUM RECEIVER

FIG. ~~50~~ 56

55

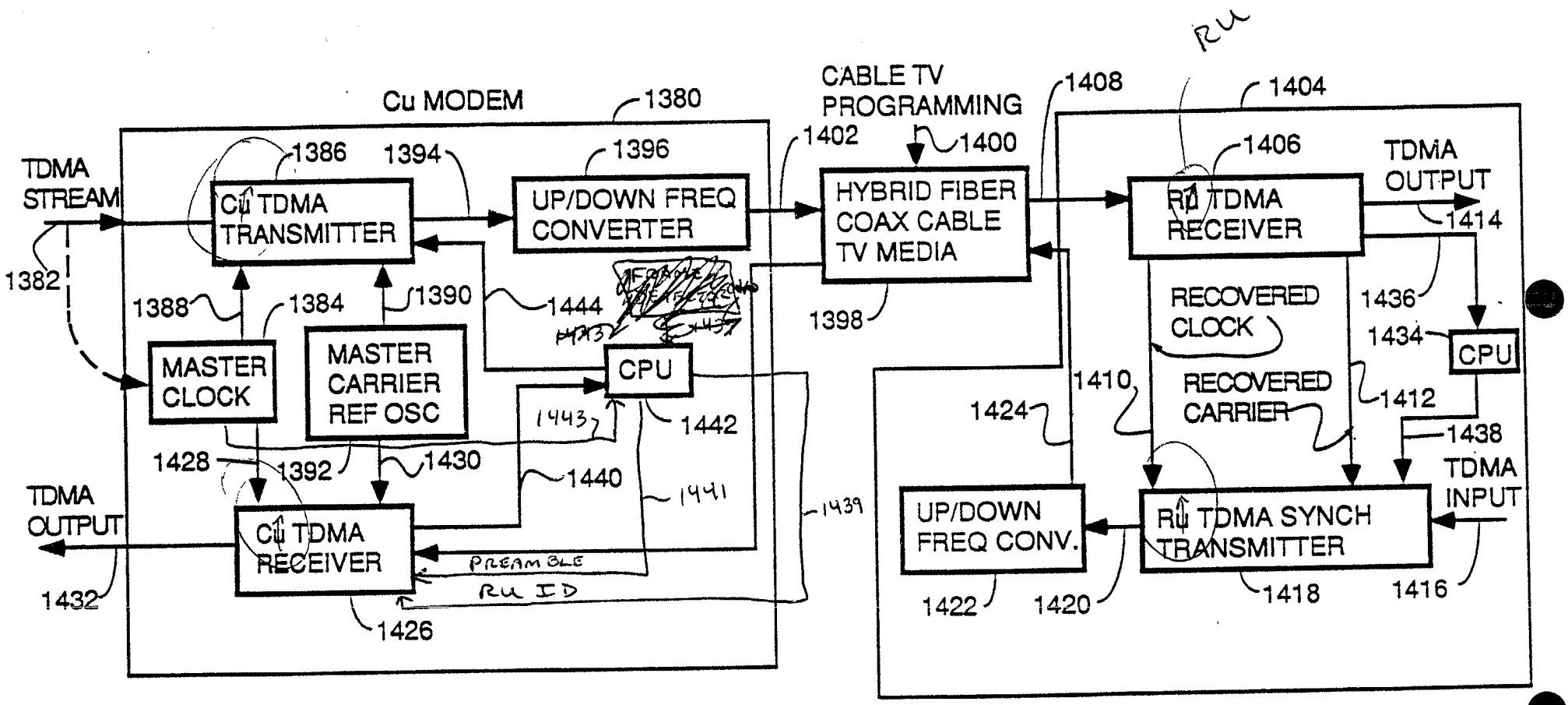


SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. 51

51

56



SYNCHRONOUS TDMA SYSTEM

FIG. 54

57

OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

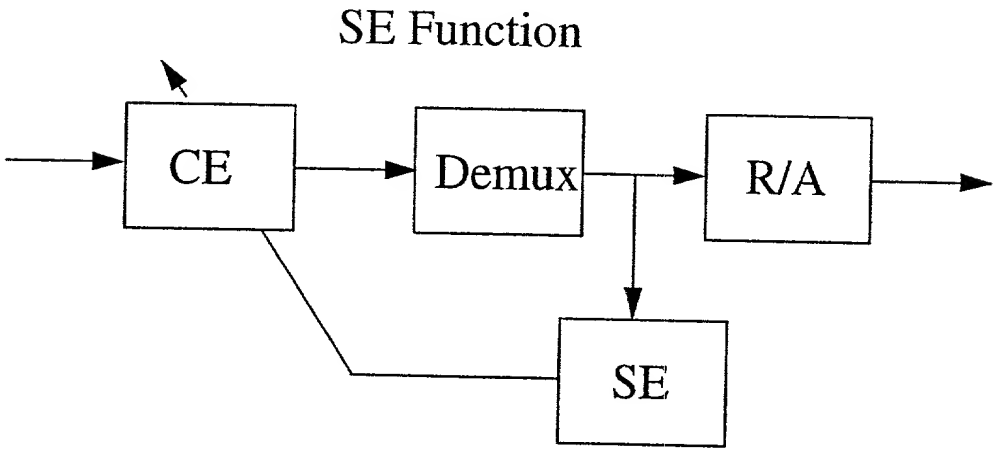
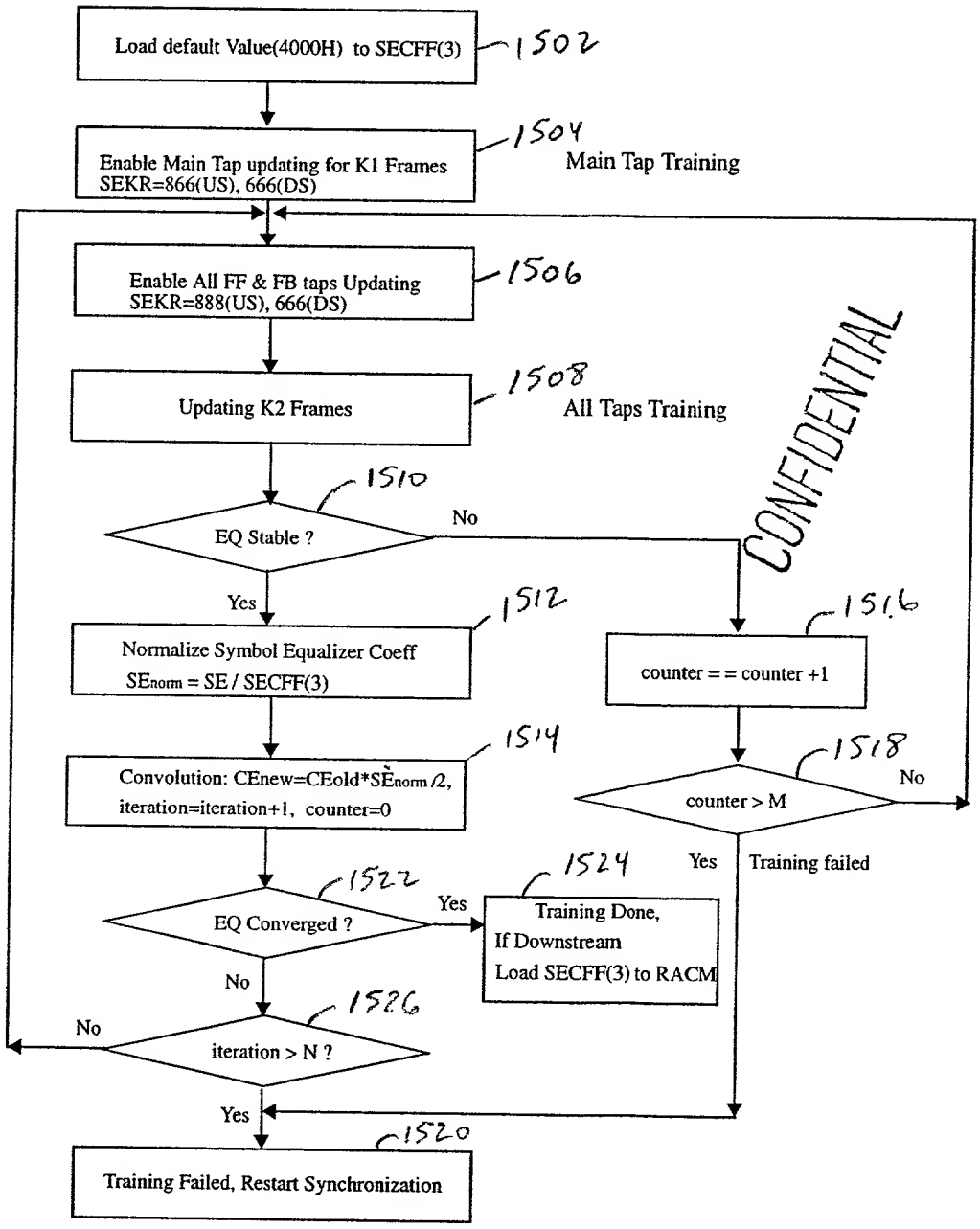


FIG. 59

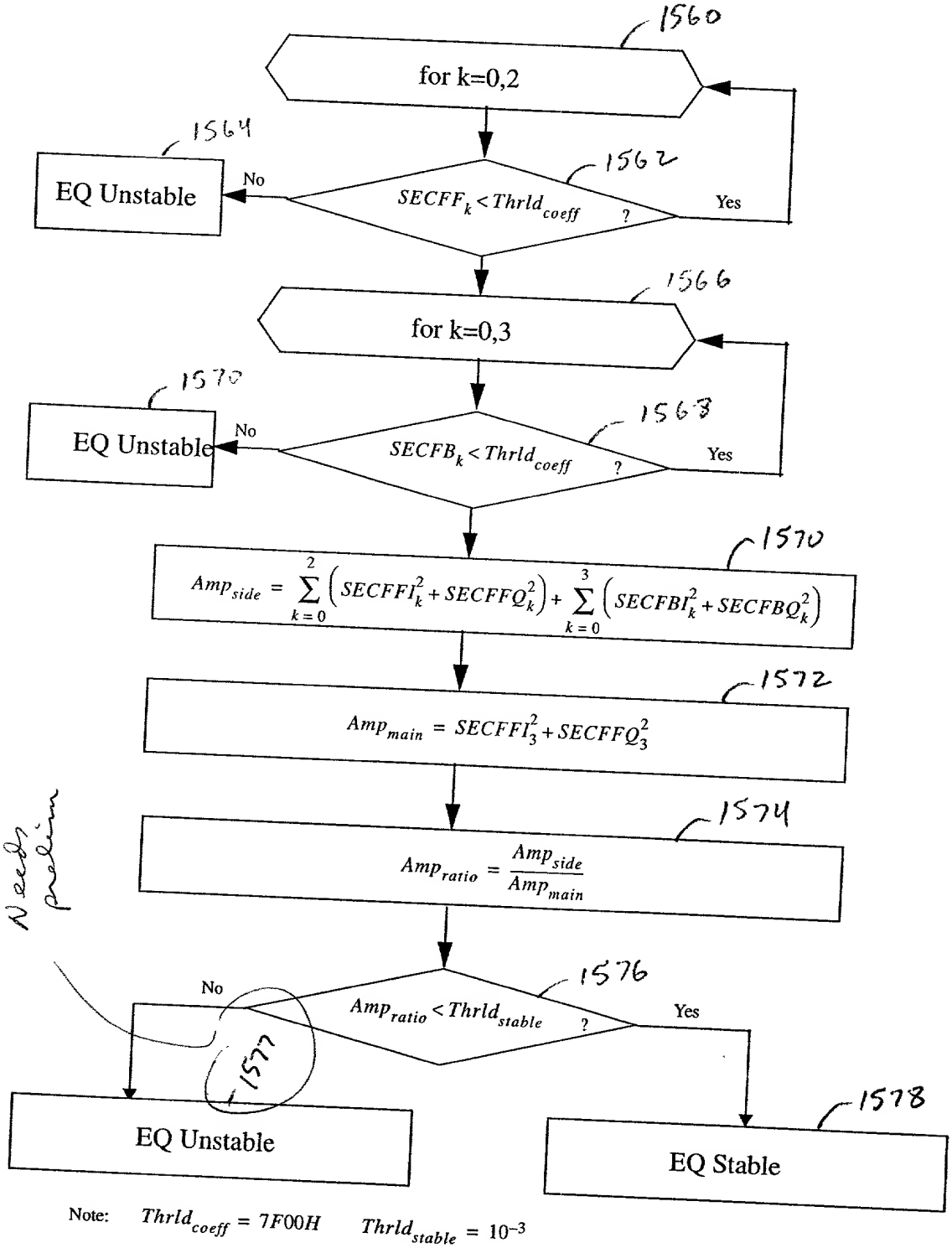
Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

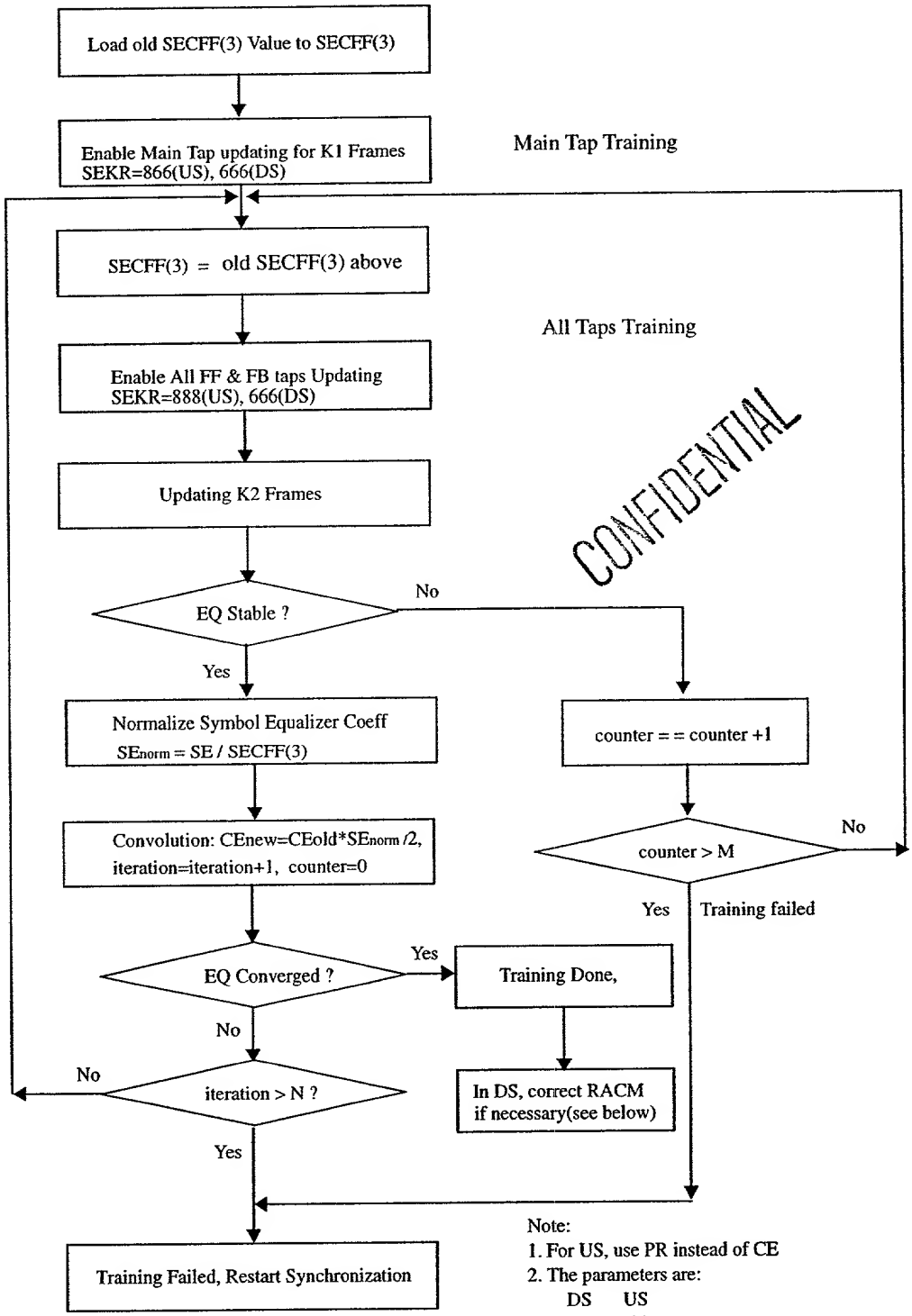
EQ Stability Check



Note: $Thrld_{coeff} = 7F00H$ $Thrld_{stable} = 10^{-3}$

FIG. 61

Periodic 2-Step Training Algorithm

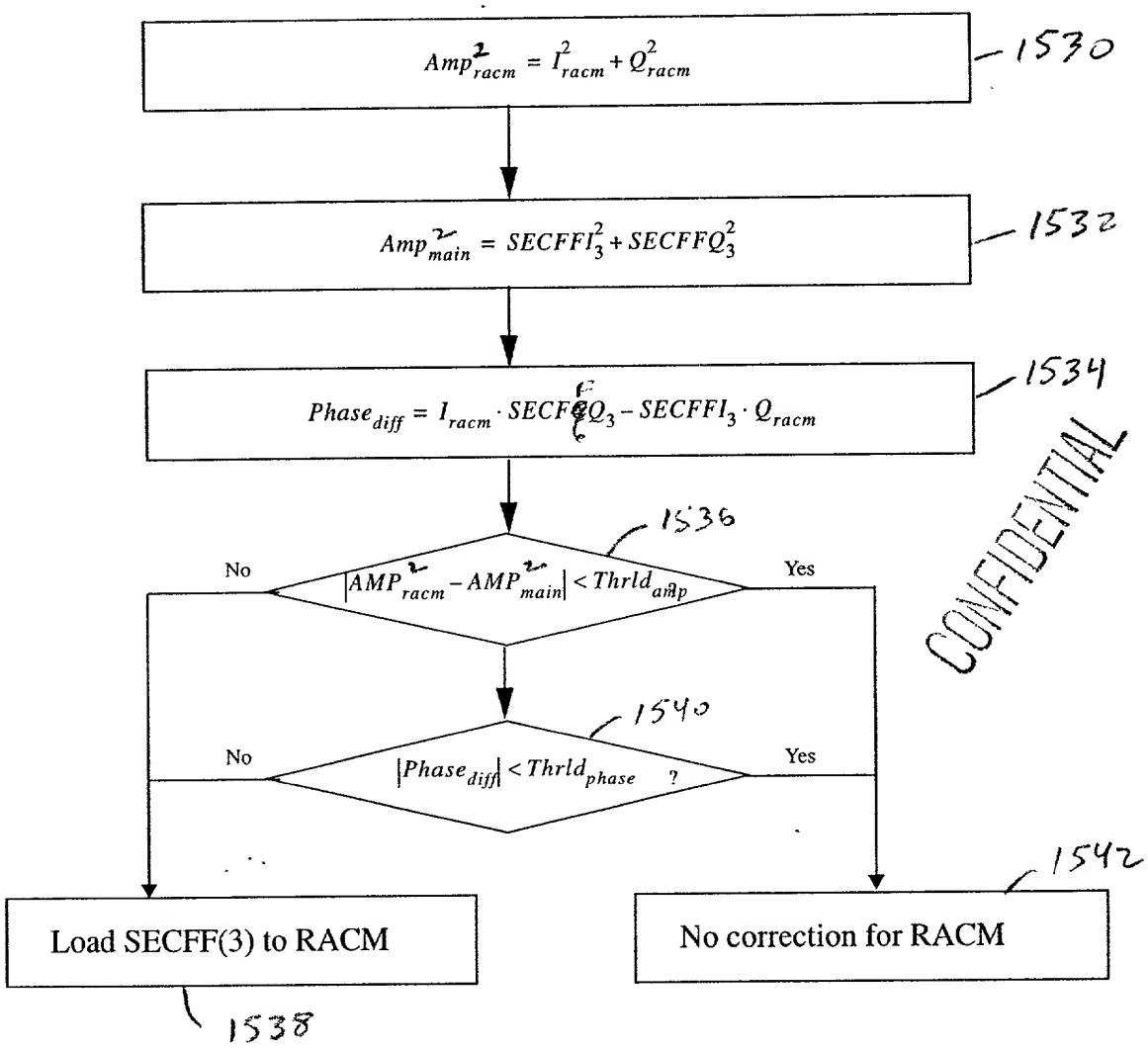


Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



CONFIDENTIAL

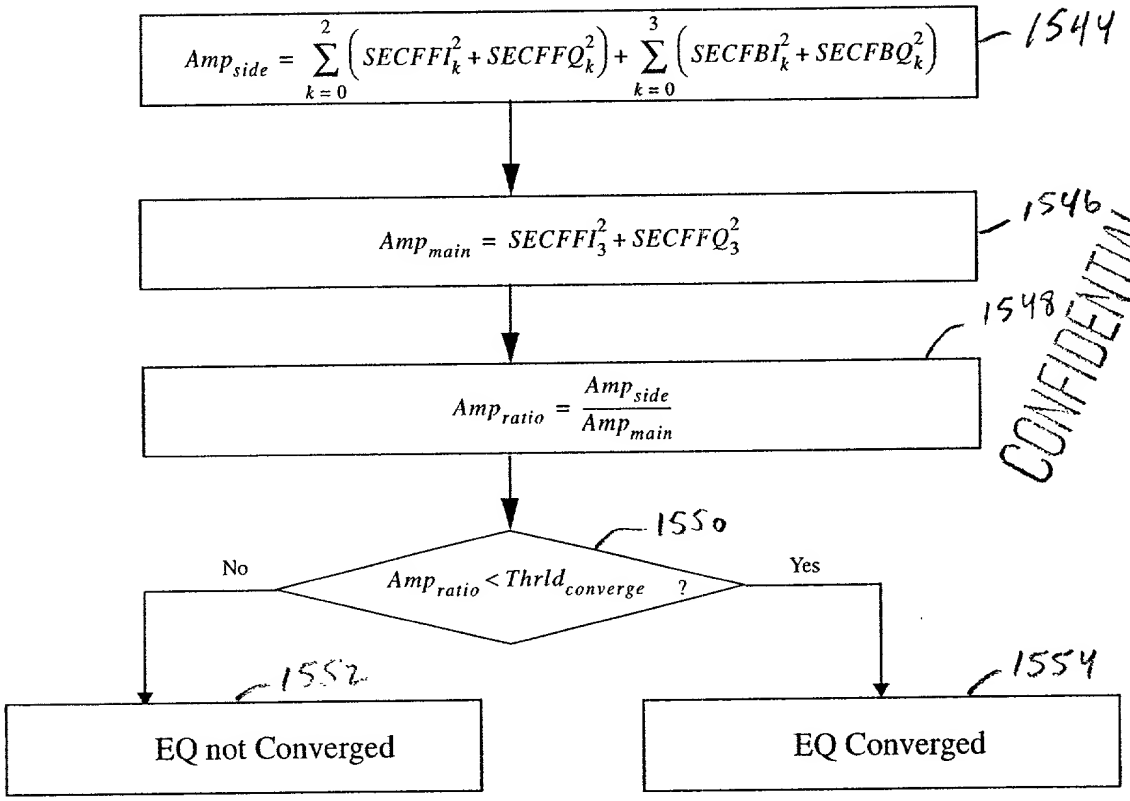
Note: $Thrld_{amp} = TBD$

$Thrld_{phase} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63.

EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart

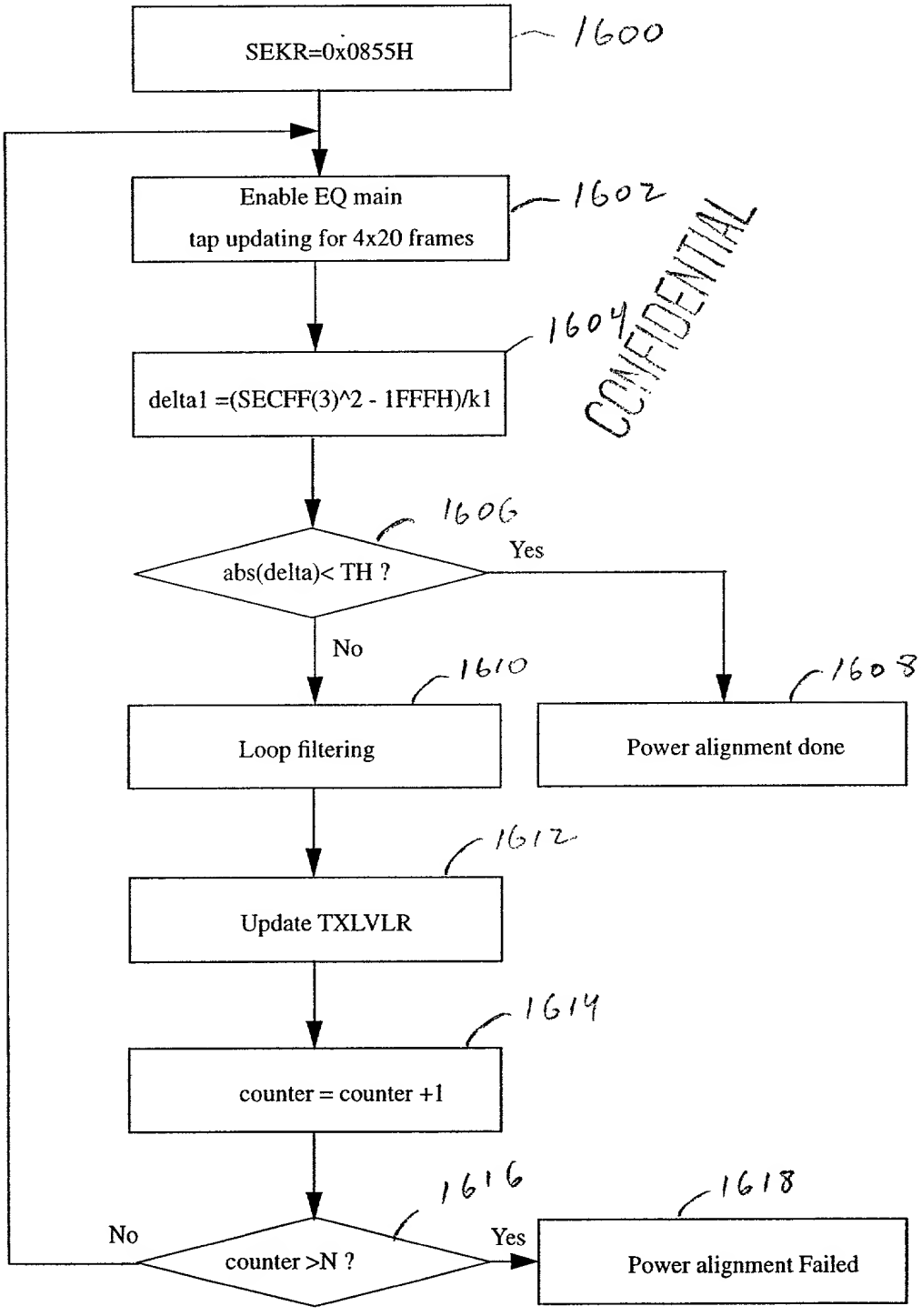


FIG. 65

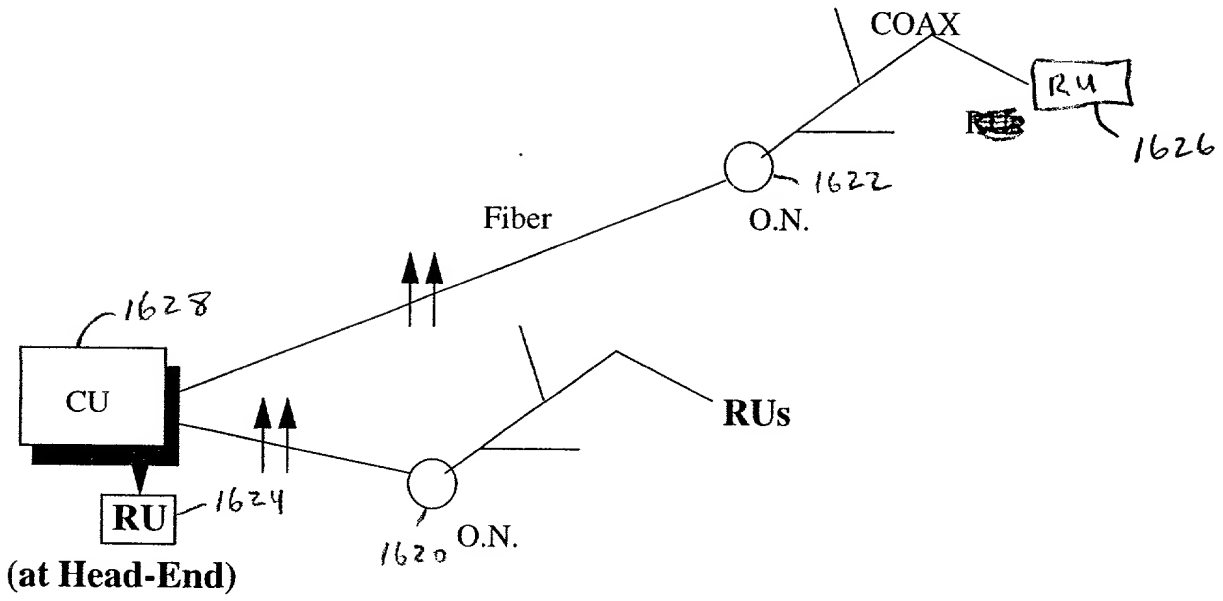
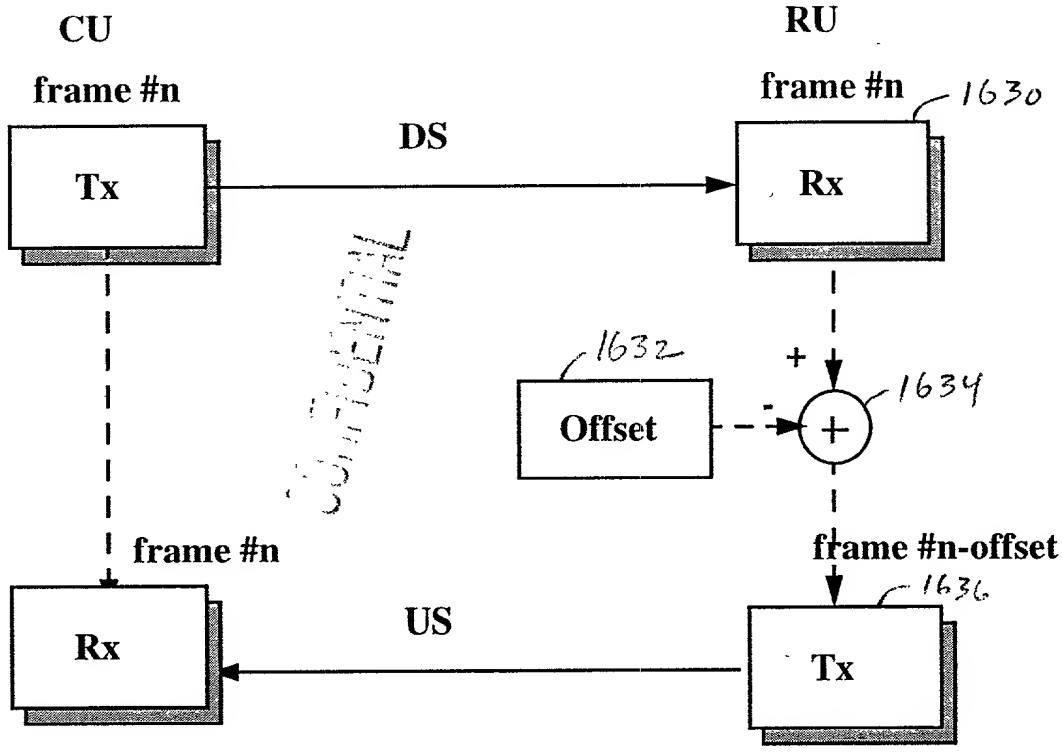


FIG. 66



Total Turn Around (TTA) in frames = Offset

FIG. 67

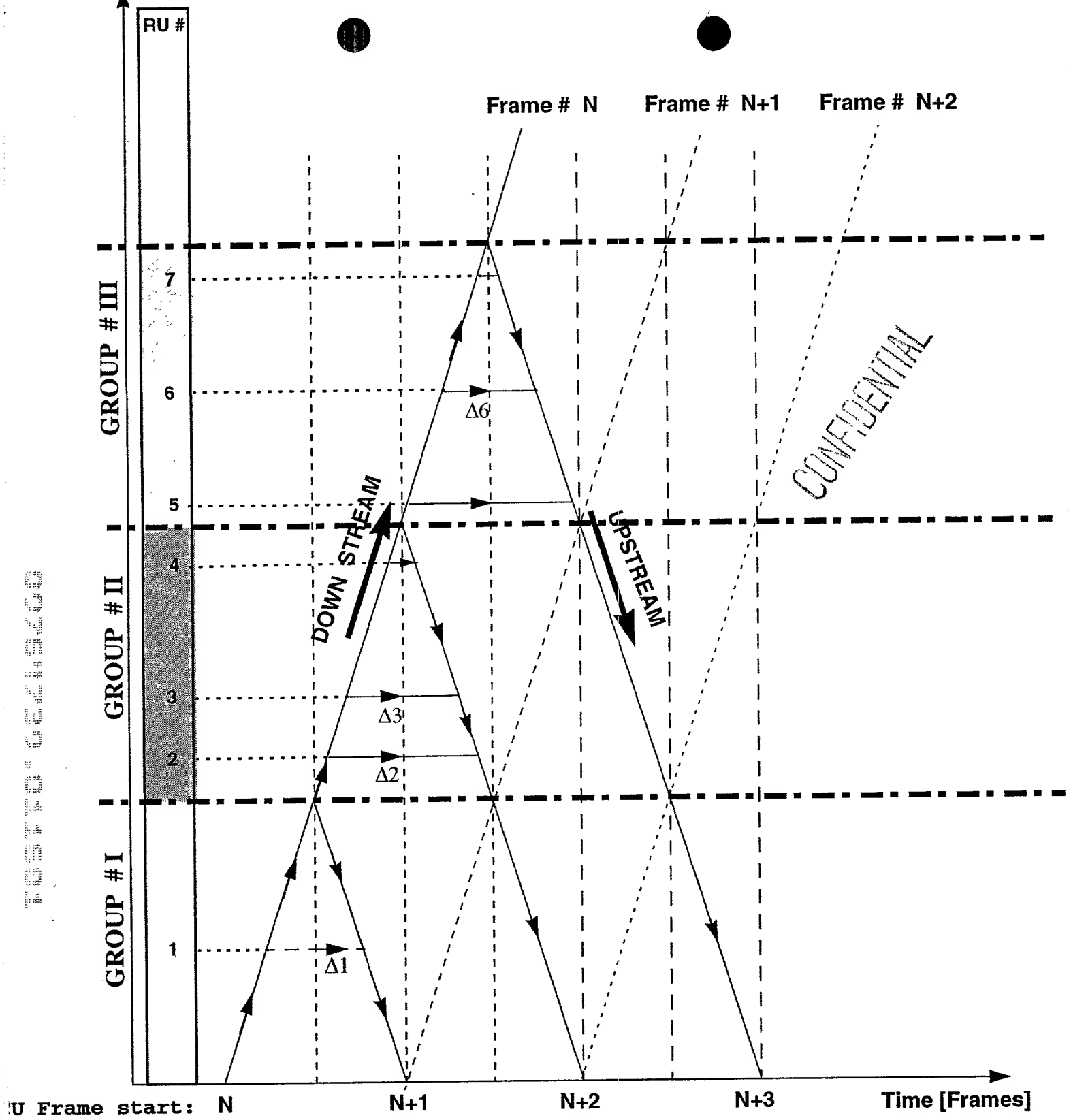


FIG. 6B

Figure 3.1: Frame start propagation along the channel

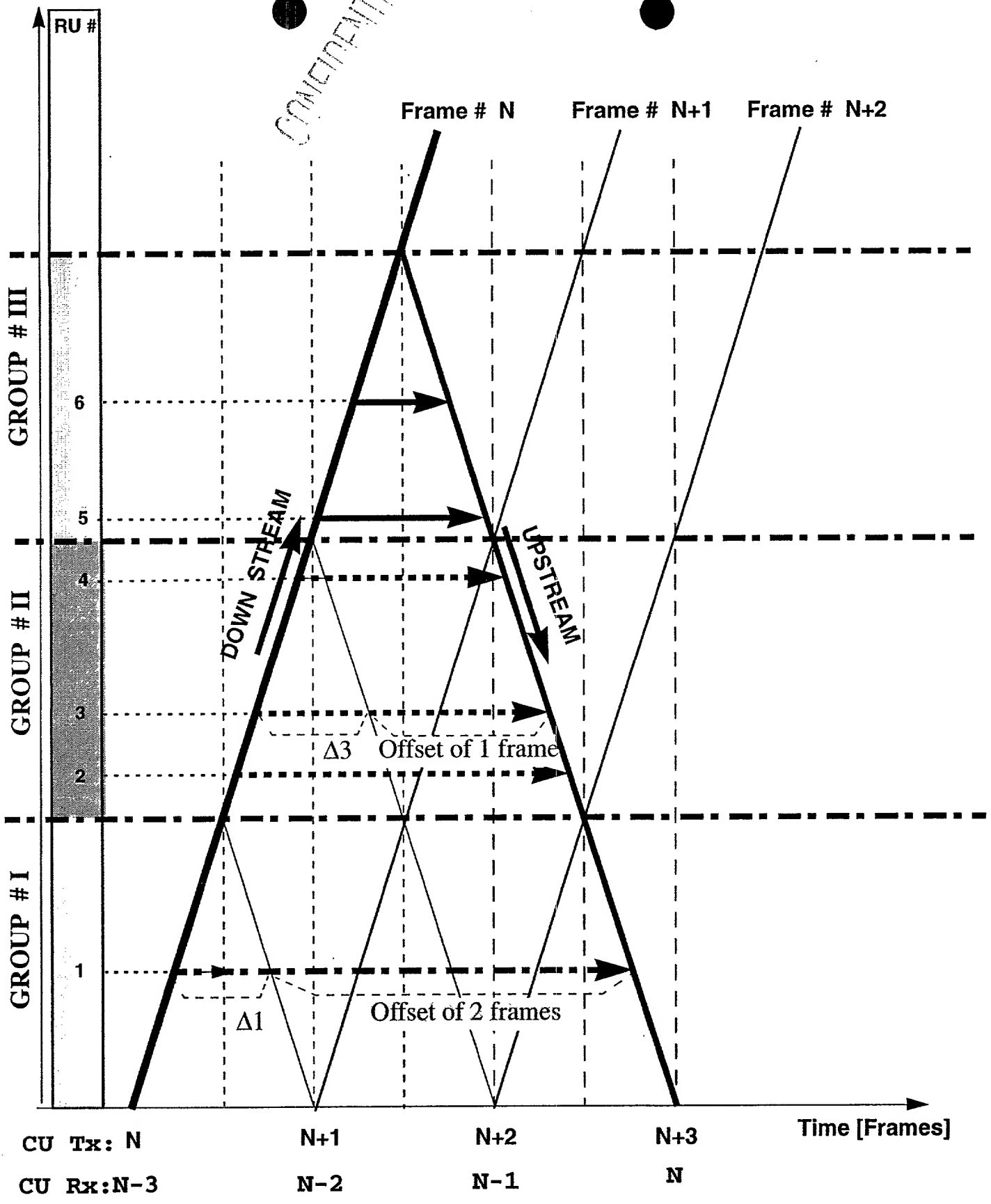


FIG. 69

Figure 69 Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

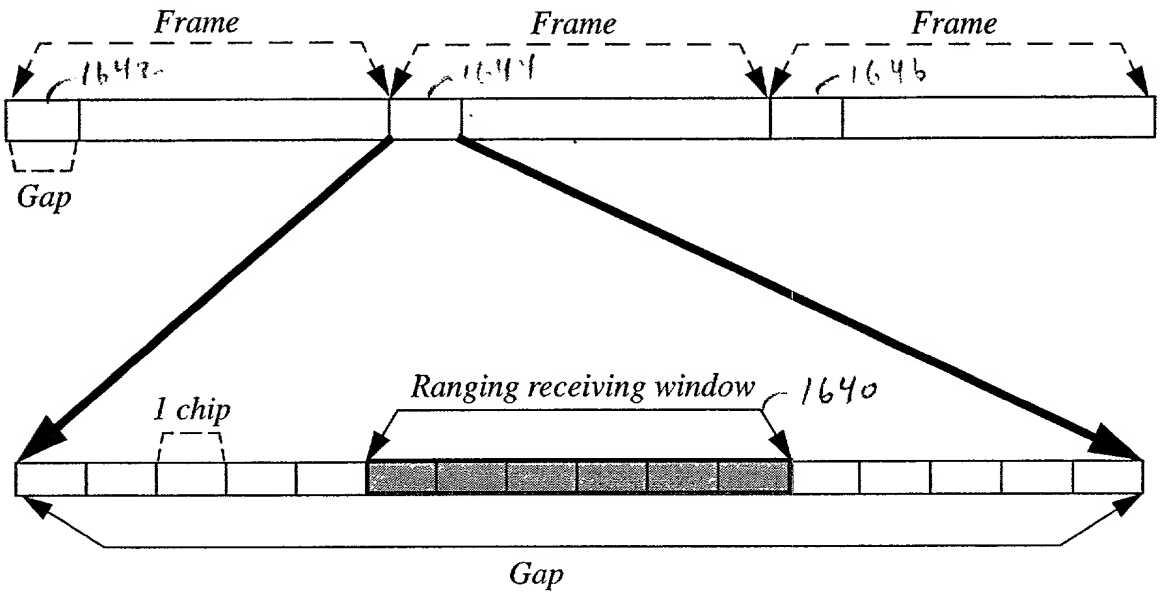

Frame
Frame
Frame
1642
1644
1646
Gap
1 chip
Ranging receiving window
1640
Gap

FIG. 7D

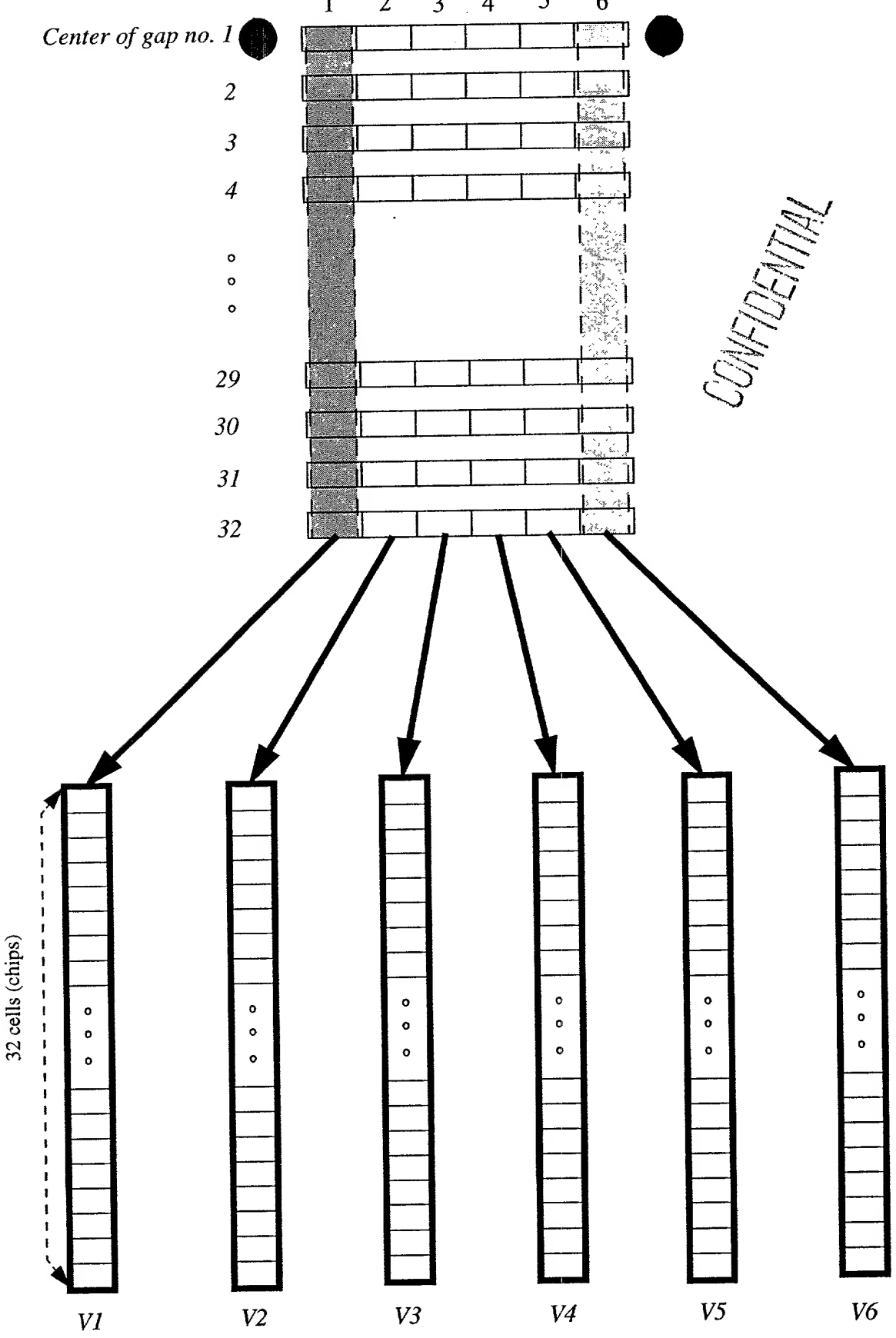


Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 71

6

Chip\FR	1	2	3	4	5	6	7		33
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**...**	**0**
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72

EQUALIZATION

CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.

1116

RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.

1118

CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.

1120

TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.

1122

AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.

IN CU

1124

CONVOLVES SE CIRCUIT WITH OLD

~~RU~~ SETS FINAL FFE & DFE COEFFICIENTS ~~INTO~~ PRECODE FFE/DFE FILTER IN TRANSMITTER AND LOAD NEWLY CALCULATED COEFFICIENTS INTO RU XMTR PRECODE FILTER

RU

TRANSPARENCY VALUES

1126

CU SETS COEFFICIENTS OF PFE 765 AND DFE 820 TO ~~ONE~~ FOR RECEPTION OF UPSTREAM PAYLOAD DATA.

54B

FIG. 45B

53B

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DI MUELLER
10/25/00
(909) 596-3733

FROM FIG. 45B

DOWNSTREAM EQUALIZATION

1128

CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

1130

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

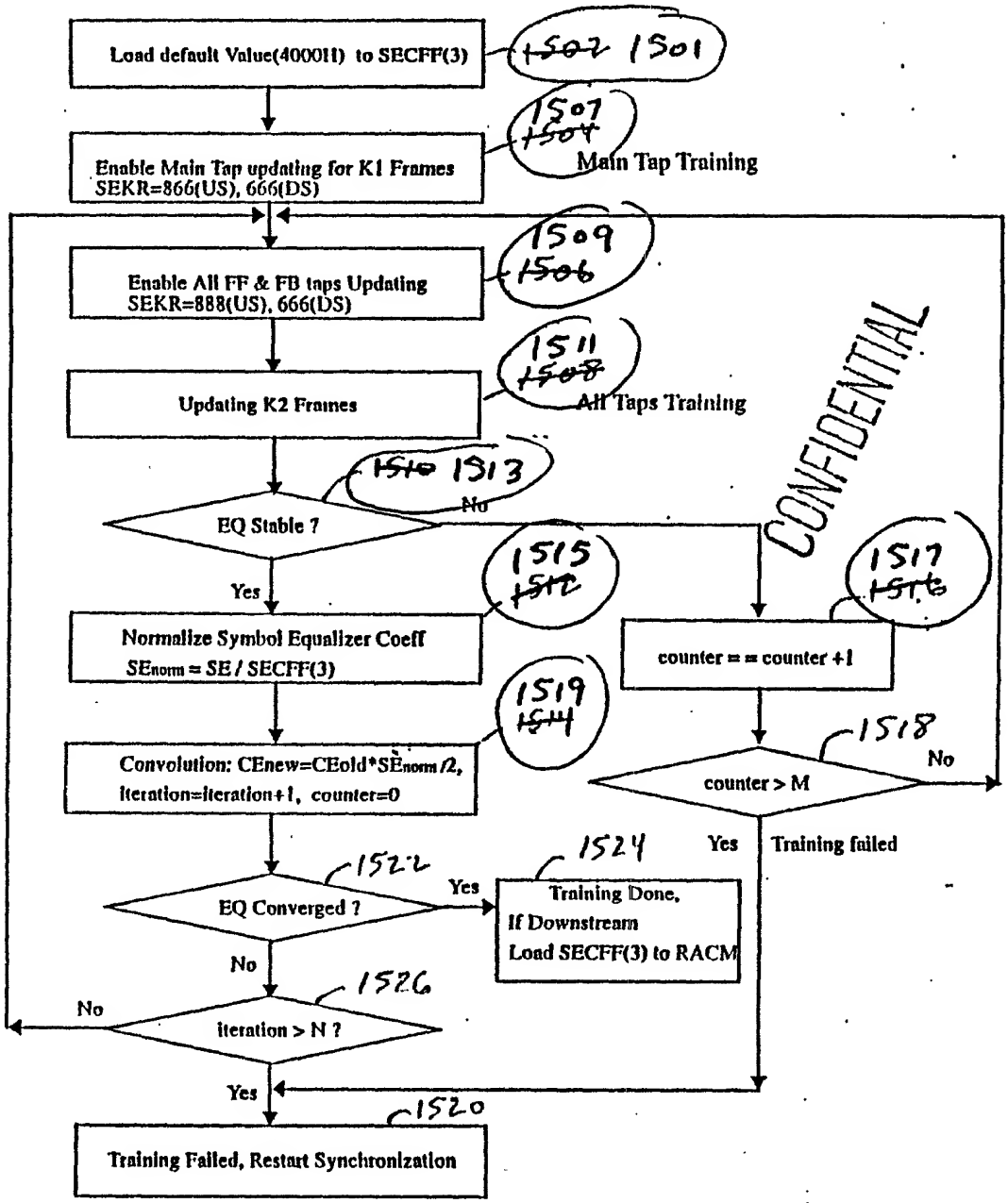
1132

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND ~~LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764~~; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AN DFE FILTERS O CE CIRCUIT 764 AND LOADS THE NEWLY CALCUL ED TAP WEIGH INTO THE FFE AND DFE FILTERS OF THE CE CIRCU

~~54C~~
FIG. ~~45C~~
53C

Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60